NAVAL POSTGRADUATE SCHOOL

MONTEREY, CALIFORNIA

THESIS

STABILITY ANALYSIS OF A CONSTANT POWER LOAD SERVICED BY A BUCK CONVERTER AS THE SOURCE IMPEDANCE VARIES

by

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September 2012

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REPORT DOCUMENTATION PAGE			Form Approved OMB No. 0704-0188
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instruction, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188) Washington DC 20503.			
1. AGENCY USE ONLY ***(Leave blank)***	**2. REPORT DATE** September 2012	**3. REPORT TYPE AND DATES COVERED** Master's Thesis	
4. TITLE AND SUBTITLE Stability Analysis of a Constant Power Load Serviced by a Buck Converter as the Source Impedance Varies		**5. FUNDING NUMBERS**	
6. AUTHOR(S) George J Roth			
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Naval Postgraduate School Monterey, CA 93943-5000		**8. PERFORMING ORGANIZATION REPORT NUMBER**	
9. SPONSORING /MONITORING AGENCY NAME(S) AND ADDRESS(ES) N/A		**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**	
11. SUPPLEMENTARY NOTES The views expressed in this thesis are those of the author and do not reflect the official policy or position of the Department of Defense or the U.S. Government. IRB Protocol number _____N/A_____.			
12a. DISTRIBUTION / AVAILABILITY STATEMENT Approved for public release; distribution is unlimited		**12b. DISTRIBUTION CODE** A	

13. ABSTRACT (maximum 200 words)

As the NAVY moves forward with plans to become less dependent on fossil fuels and more dependent on hybrid electric drives and all-electric ships, being aware of the stability issues associated with direct current (DC)-DC and DC-alternating current (AC) power converters and understanding how to solve the issues that come with using them, are very important. The negative input impedance that is observed when using a buck converter servicing a constant power load (CPL) is one of the issues that needs to be understood. Understanding the stability issue caused by the negative input impedance and mitigating this instability by varying the input source impedance is the focus of this thesis.

Using a Simulink model of an ideal CPL, we determined the expected results. Then, the Simulink results were compared to the analysis of the linearized small signal transfer function to determine how well the results of the two matched. Finally, the hardware model was observed and its results compared to the Simulink model and linearized small signal transfer function.

These experiments led to the conclusion that increasing the capacitance or decreasing the inductance reduces the input source impedance and, ultimately, reduces instability in the system.

14. SUBJECT TERMS Constant Power Load, Buck Converter, DC—DC, Negative Impedance, Stability			**15. NUMBER OF PAGES** 71
			16. PRICE CODE
17. SECURITY CLASSIFICATION OF REPORT Unclassified	**18. SECURITY CLASSIFICATION OF THIS PAGE** Unclassified	**19. SECURITY CLASSIFICATION OF ABSTRACT** Unclassified	**20. LIMITATION OF ABSTRACT** UU

NSN 7540-01-280-5500 Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18

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STABILITY ANALYSIS OF A CONSTANT POWER LOAD SERVICED BY A BUCK CONVERTER AS THE SOURCE IMPEDANCE VARIES

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Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
September 2012

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ABSTRACT

As the NAVY moves forward with plans to become less dependent on fossil fuels and more dependent on hybrid electric drives and all-electric ships, being aware of the stability issues associated with direct current (DC)-DC and DC-alternating current (AC) power converters and understanding how to solve the issues that come with using them, are very important. The negative input impedance that is observed when using a buck converter servicing a constant power load (CPL) is one of the issues that needs to be understood. Understanding the stability issue caused by the negative input impedance and mitigating this instability by varying the input source impedance is the focus of this thesis.

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LIST OF ACRONYMS AND ABBREVIATIONS

AC	Alternating Current
C	Capacitor
Cap	Capacitor
C_f	Filter Capacitor
CPL	Constant Power Load
dB	Decibel
DC	Direct Current
DC ZEDS	DC Zonal Electrical Distribution System
EV	Electric vehicles
FCV	Fuel Cell Vehicle
HEV	Hybrid Electric Vehicle
Hf	Final Load Transfer Function
Hf_vec	Final Load Transfer Function Vector
Hi	Initial Load Transfer Function
Hi_vec	Initial Load Transfer Function Vector
I	Current
Ind	Inductor
I_S	Source Current
KVL	Kirchhoff Voltage Law
L_S	Source Inductance
MEV	More Electric Vehicle
MVDC	Medium Voltage DC

P	Power
P_O	Output Power
Pof	Final Power Level
Poi	Initial Power Level
R	Resistance
R_1	Resistor one
R_2	Resistor two
R_S	Source Resistance
SMC	Sliding Mode Controller
V	Voltage
V_{DC}	Direct Current Voltage
V_O	Output Voltage
V_{OO}	Nominal DC Output Voltage
V_{SO}	Nominal Source Voltage
ΔV_O	Small Signal Variation in Output Voltage
ΔV_S	Small Signal Variation in Source Voltage

EXECUTIVE SUMMARY

As the NAVY moves forward with plans to become less dependent on fossil fuels and more dependent on hybrid electric drives and all-electric ships [1], being aware of the stability issues associated with direct current (DC)-DC and DC-alternating current (AC) power converters and understanding how to solve the issues that come with using them are very important. The negative input impedance that is observed when using a buck converter servicing a constant power load (CPL) is one of the issues that needs to be understood. Understanding the stability issue caused by the negative input impedance and mitigating this instability by varying the input source impedance is the focus of this thesis.

The objective of this thesis was to observe the expected behavior of a buck converter acting as a CPL as the source impedance changed. Much work has already been done in the area of controlling power converters acting as CPLs, but not much literature could be found on how the input impedance affects the converters when servicing a CPL.

The first step of this thesis was to understand the idealized Simulink model of CPLs designed by Prof. Alexander Julian and the small signal voltage transfer function [2].

The goal was to use the Simulink model and small signal voltage transfer function to predict the behavior of the system's stability and see how varying the values of the components makes a difference in stability. The second step was to build a hardware model to see how a buck converter acting as a CPL really is affected when the input source impedance changes and to see how accurately the ideal Simulink model and linearized equation predicts the hardware results. A simple circuit was built in the lab using the Power-one module model DFA6U12S5, which is a buck converter acting as a CPL.

A buck converter is a step down converter: it takes the input voltage and reduces the voltage so that the output voltage is lower than the input. A buck converter is a simple

circuit consisting of a source, two switches (usually a transistor and a diode), an inductor, a capacitor, and a load. Power converters such as a buck converter are used because of their precise output voltage control capability [3], which enables them to respond almost immediately to system changes. This advantage of the buck converter is a disadvantage when it acts as a CPL. The Buck converter power converter has an input voltage range between 9 V and 27 V and outputs 5 V DC.

Constant power loads create a destabilizing effect in the circuits to which they are connected because of negative impedance instability [1],[3]-[7]. This negative impedance comes from the way the input voltage and current respond when a load change occurs in a CPL. When voltage decreases, current increases; and when voltage increases, current decreases. This change in voltage or current is the destabilizing effect of a CPL.

Using a Simulink model of an ideal CPL, we determined what the expected results should be. Then, comparing the Simulink results to the analysis of the linearized small signal transfer function, we analyzed how well the results matched.

A simple model was constructed in order to compare the simulation results with the experimental results. A PROTO-BOARD PB-503 was used for the construction of the circuit, and the built-in power source was used as the source. Two capacitors, two inductors, and two resistors were obtained from the lab, and the Power-one module was used as the buck converter.

In this thesis the characteristic trait of tightly regulated power electronics, which allow them to act like CPLs and the stability issues concerning CPLs, were reviewed.

The results observed show that the models accurately predicted the frequency of the disturbance on the bus feeding the CPL of the hardware experiment at the initial load. The amplitude was not accurately predicted at either load, but the trend was similar for the Simulink model, the linearized small signal transfer function and the hardware model. The frequency at the final load was also not accurately predicted, but again the same trend was seen in all methods of analyses. The Buck converter's control scheme is not known; this unknown factor may explain the inaccurate prediction at higher loads.

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ACKNOWLEDGMENTS

First off I need to give thanks to the Lord, who has blessed me with the opportunity to attend the Naval Postgraduate School. Thank you for the perseverance to get through the past two years of classes, and to get through the thesis process.

I would like to express my gratitude to all the faculty and staff who have helped make this tour a successful one. Thank you to Alice Lee, the Electrical Engineering Educational Technician who keeps everything together, and who always had time to help me with my administration questions. In particular, I would like to express my appreciation to my thesis advisor Professor Julian. Thank you for being willing to advise me, knowing that I would need a little extra help and explanation compared to the average student. I appreciate your time and advice through the whole thesis process.

Finally, I have to thank the most important people in my life. To my loving and beautiful wife, Stacy: you have been so gracious and supportive towards me from the moment we began this adventure. I appreciate all your help with school work, your motivational pep talks, and your never-ending support and encouragement. Thank you for taking such great care of our children. Knowing that you were at home with them allowed me to put in the late nights necessary to get me through this Masters program.

To Dawn and George: I love you very much. Spending time with you has constituted some of my favorite memories in Monterey. I love seeing how you grow and learn new things every day.

To my parents and in-laws: thank you for always loving me and believing in me. Thank you for your support in whatever ways Stacy and I have ever needed.

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I. INTRODUCTION

A. BACKGROUND

Since the introduction of power electronics there have been new uses for direct current (DC)-DC converters in many fields of electronics. People use power converters because of an important characteristic that tightly regulated power converters exhibit. This characteristic is an almost-perfect regulation at the output terminals that is independent of the changes made at the input terminals [1]. Because of this important characteristic, power electronics-based power supplies are finding their way into environments such as aircrafts, vehicles and ships [1]. The benefit of a constant output that does not depend on input changes does have associated problems. A tightly regulated, almost perfect power converter has a characteristic at the input terminals that reflects a constant power load (CPL) [1]. CPLs have a negative impedance characteristic at the input terminals which can have an effect on the stability of the system [1], [2].

As the NAVY moves forward with plans to become less dependent on fossil fuels and more dependent on hybrid electric drives and all-electric ships [3], being aware of the stability issues associated with DC-DC and DC-alternating current (AC) power converters, and understanding how to solve the issues that come with using them, are very important. The negative input impedance that is observed when using a buck converter servicing a CPL is one of the issues that needs to be understood. Understanding the stability issue caused by the negative input impedance and mitigating this instability by varying the input source impedance is the focus of this thesis.

B. OBJECTIVE

The objective of this thesis was to observe the expected behavior of a buck converter acting as a CPL as the source impedance changed. Much work has already been done in the area of controlling power converters acting as CPLs, but not much literature could be found regarding how the input impedance affects the converters when servicing a CPL. After the expected behavior was observed through both simulation and hardware verification, the source impedance was changed**.** The steady state output was

observed to see the effects as the impedance changed. Comparisons between the Simulink model and the linearized equation of the ideal model were made to see how well they predicted the behavior.

C. PREVIOUS WORK

In [1] the control of a buck DC-DC converter was studied while operating with a CPL in sea and undersea vehicles. The paper primarily focused on the large signal analysis of the converter loaded by a CPL and on the design of a feedback system. The authors used a controller that was a combination of an instantaneous current feedback loop using hysteresis and a proportional-integral (PI) algorithm to regulate the output voltage of the converter.

In [2] the authors looked at CPLs and negative impedance instability in automotive systems, specifically more electric vehicles (MEVs), hybrid electric vehicles (HEVs), electric vehicles (EVs), and fuel cell vehicles (FCVs). The author's focus was on the negative impedance instability concept of CPLs in advanced multiconverter automotive power systems.

In [3] we see another article focusing on the controller, with the focus on using medium-voltage DC (MVDC) integrated power systems, whose use is a goal for future surface combatants and submarines. The authors proposed a third order sliding-mode controller (SMC) for DC-DC buck converters with CPLs. The problem here is that in MVDC shipboard power systems, the DC-DC converters are used to supply constant power to electrical loads, and these loads have a negative impedance characteristic.

The last article was motivated by the Navy's interest in developing a DC Zonal Electrical Distribution System (DC ZEDS). The authors of [4] developed a DC-DC buck chopper nonlinear control law that guarantees local asymptotic stability for a range of admissible constant power.

D. APPROACH

The first step of this thesis was to understand the idealized Simulink model of CPLs and the small signal voltage transfer function [5].

The goal was to use the small signal voltage transfer function to predict the behavior of the system's stability by solving the roots of the characteristic equation and to see how varying the values of the components affects stability. The last step was to build a hardware model to see how a CPL serviced by a buck converter was affected when the input source impedance changed and to see how accurately the ideal Simulink model and linearized equation predicted the hardware results. A simple circuit was built in the lab using the Power-one converter model DFA6U12S5 as a buck converter servicing a CPL.

E. THESIS ORGANIZATION

The theory of how a tightly regulated power converter, acts like a CPL at the input terminals, the stability issues with CPLs, and possible fixes for these stability issues are discussed in Chapter II. The simulation of the ideal model, along with the hardware experiments and verifications, are discussed in Chapter III. The results and analysis of the simulations and hardware experiments are presented in Chapter IV. Conclusions are drawn based on the results from the simulations and hardware experiments in Chapter V. The validity of the Simulink model is reviewed. Possibilities for future work in this topic are also presented.

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II. CONSTANT POWER LOAD SERVICED BY A BUCK CONVERTER

A buck converter is a step down converter: it takes the input voltage and reduces the voltage so that the output is lower than the input. A buck converter is a simple circuit consisting of a source, two switches (usually a transistor and a diode), an inductor, a capacitor, and a load. Figure 1 is an example of a simple buck converter circuit. Power converters such as a buck converter are used because of their tight output voltage control capability [1], which enables them to respond almost immediately to system changes. This advantage of the buck converter is a disadvantage when it acts as a CPL. In this thesis the Power-one power converter was used during lab experiments. The Power-one has an input voltage range between 9 V and 27 V and outputs 5 V DC. A buck converter regulates the output capacitor voltage (voltage across *C* in Figure 1) by controlling the duty cycle of the transistor shown in Figure 1. This is accomplished by closing a control loop from the output voltage to the transistor base. Typically the output voltage is held constant independent of the input voltage. This causes the power consumed by R_{load} to be constant, and therefore, the buck converter looks like a CPL.

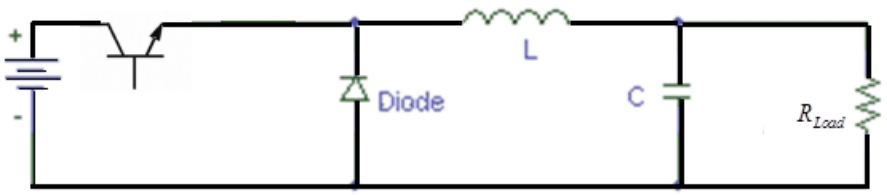

Figure 1. Buck converter diagram.

A. CONSTANT POWER LOAD

In a CPL, the load maintains a constant power level by drawing more or less current as required by the situation. For example, if the input voltage decreases, the input current increases; or if the input voltage increases, the input current decreases in order to maintain a constant power level. This trait of a CPL is a "destabilizing effect known as negative impedance instability" [2].

B. HOW A BUCK CONVERTER ACTS LIKE A CONSTANT POWER LOAD

A buck converter acts as a CPL at the input terminals because of the way the load appears across the output terminals. A couple of basic equations are necessary to mathematically explain the way the load appears. From Ohm's Law, $V = IR$ where V is voltage, I is current and R is resistance. Power P is given by $P = IV$ and measured in Watts (W). Substituting Ohm's Law into the power equation, we get

$$P = \frac{V^2}{R} \tag{1}$$

which was used to measure the load. Because of the tight output voltage regulation of the power converter, the output voltage is held constant at 5 V DC. When the load V^2/R increases because R decreases, the power converter requires more input current in order to maintain the constant output voltage. A load is generally thought of as a resistance, and when resistors are added in parallel, the total resistance decreases because of:

$$\frac{1}{R_T} = \frac{1}{R_1} + \frac{1}{R_2} + \bullet\bullet\bullet + \frac{1}{R_n} \tag{2}$$

where R_n is the nth resistor.

Because the voltage output of the buck converter is not going to change–in other words, it maintains a constant 5 V DC at the output terminals–the only way to change the load or power level in equation (1) is to change the resistor value. As the load changes, the power level changes, and the stability at the input terminal of the buck converter is affected. Again, a CPL is a characteristic that is created when using power electronics, and the almost perfect regulation [1] of the power electronics is the cause for the negative instability effect. Figure 2 is an example of a buck converter. Closing a control loop on v_O makes the buck converter act like a CPL.

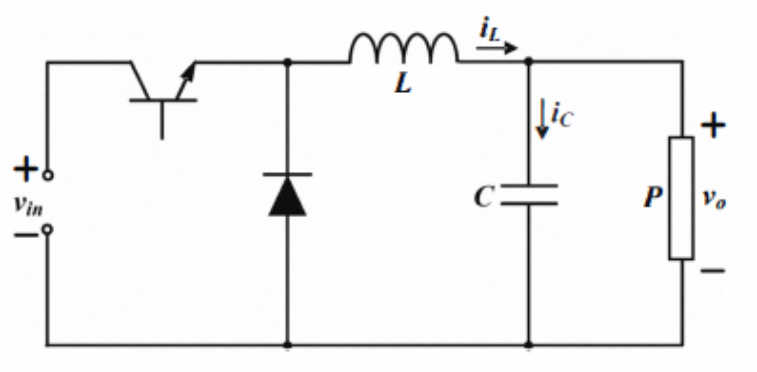

Figure 2. A buck converter with a constant-power load (From [3]).

C. STABILITY ISSUES WITH CPLS AND POSSIBLE SOLUTIONS

Constant power loads create a destabilizing effect in the circuits they are connected to because of negative impedance instability [1]–[4], [6], [7]. This negative impedance comes from the way the input voltage and current respond when a load change occurs in a CPL. When voltage decreases and current increases, or vice versa, this change in voltage or current is the destabilizing effect of a CPL.

One possible fix is to not control them as tightly; doing so, however, can cause other issues because the control is tightly regulated so that a constant voltage or current is maintained at some point of interest. Another fix is to put a decoupling or calming capacitor in parallel with the source before the power converter. We show in the results section how our original simulation and hardware experiment acted with our initial capacitor value and then show how it was affected when we increased the capacitance. The result is that the steady state input voltage to the buck converter had a smaller ripple because it was more stable with a larger capacitance. The increase in capacitance also decreased the turn-on transient and the ripple seen after the load change. Reducing the source inductance is another helpful remedy. When decreasing the source inductance, the circuit reacted similarly to the way it does when the capacitance is increased. When decreasing the inductance or increasing the capacitance, the source impedance is ultimately lowered. The lowering of the source impedance has a positive effect on the circuit from the standpoint of stability.

Placing a coupling capacitor or filter capacitor (C_f) in parallel with the source and the power converter is important because the capacitor makes a significant difference. The larger capacitance in my simulations and experiment made a significant difference in decreasing the ripple as mentioned above. The decreased ripple is important because a marginally stable device does not break down a device such as a microprocessor immediately, and a 1-volt ripple voltage has more negative long-term effects on the equipment's life expectancy than a smaller ripple voltage.

When a smaller inductor was placed in the circuit, or when the inductor was eliminated (as by shorting the one in the circuit), the ripple voltage was significantly reduced. It is also important to realize that the distance between the CPL and the inductor and capacitor has a distinct effect on the circuit because impedance in cables or electric lines builds over distance. In short, the inductor and capacitor need to be as close to the CPL as possible.

In this chapter, a particular power electronics device called a buck converter was introduced and how it acts like a constant power load was discussed. The stability issues with CPLs were reviewed, and a few ideas were mentioned on how to help make a circuit with a CPL more stable. The methods used to analyze the system in simulation, analytically and in a hardware example are discussed in the next chapter.

III. SIMULATION AND HARDWARE MODEL.

Using a Simulink model of an ideal CPL, we determined the expected results. Then, comparing the Simulink results to the results of the analysis of the linearized small signal transfer function, we analyzed how well the results matched. Finally, observing the hardware model and comparing its results to the Simulink model and linearized small signal transfer function, we see that the Simulink model predicts the behavior of a CPL. The Simulink model predicted the frequency of the system, but it did not match the amplitude seen in the hardware experiment. This difference between the simulation and hardware experiment is likely due to the unknown control mechanism that the buck converter uses to maintain a constant voltage. This model is useful because it provides a better understanding of how the input impedance affects the stability of a CPL.

A. IDEAL CONSTANT POWER LOAD

An ideal Simulink Model of a CPL, shown in Figure 3 [6], was studied in order to understood how a CPL functions. The Simulink model shown in Figure 4 was developed using the circuit in Figure 3.

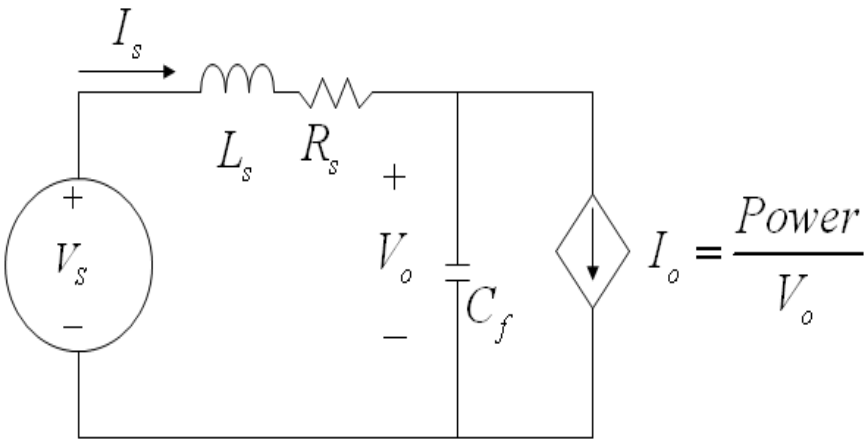

Figure 3. Circuit example with a CPL (From [5]).

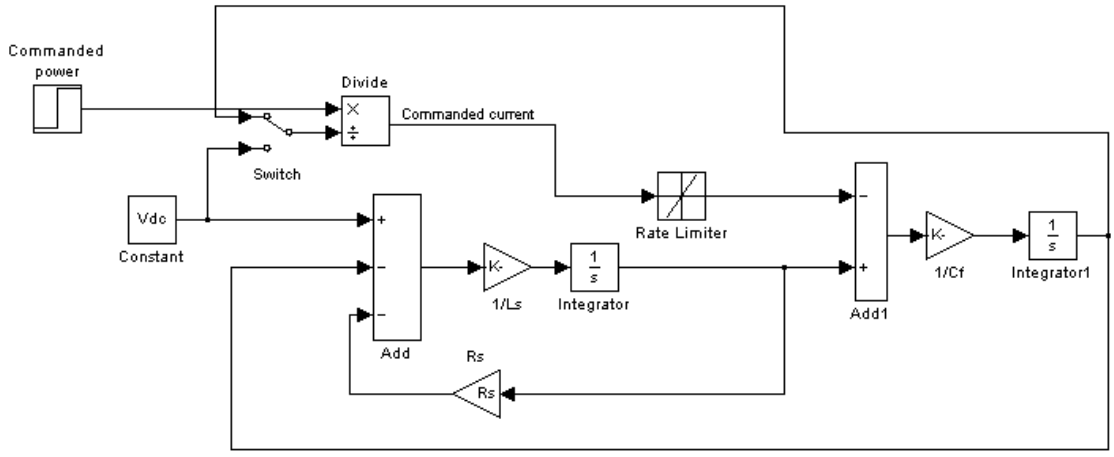

Figure 4. Block diagram of Simulink model for ideal constant power load (From [5])

The Simulink model in Figure 4 is an idealized CPL developed from the circuit in Figure 3. The Simulink model demonstrated the unwanted consequences of a CPL. The simulation showed that, after a load change, the voltage decreased and the current increased just as one would expect a CPL to act. Only the voltage response was considered in this thesis; however, as voltage decreases, current increases, and vice versa.

B. USING THE LINEARIZED EQUATION WITH MATLAB TO PREDICT STABILITY

One way to better understand how a CPL behaves is by stepping through the derivation of the small signal voltage transfer function and developing the linearized model of the idealized CPL which allows for analysis of the characteristic equation. Using Figure 3, Kirchhoff's Voltage Law (KVL) and the Taylor series expansion in order to linearize the nonlinear equation, we obtain the Laplace domain equations which lead to the small signal voltage transfer function where V_S is the source voltage, s is the Laplace operator, L_S is the source inductance, R_S is the source resistance, I_S is the source current and V_O is output voltage:

$$V_S = \left(sL_S + R_S\right) I_S + V_O \tag{3}$$

and

$$I_S = sC_f V_O + \frac{P_O}{V_O} \tag{4}$$

where P_O is the output power. Substituting (4) into (3), we get

$$V_S = \left(sL_S + R_S\right)\left(sC_f V_O + \frac{P_O}{V_O}\right) + V_O . \tag{5}$$

Simplifying, we get

$$V_S = s^2 L_S C_f V_O + sR_S C_f V_O + s\frac{L_S P_O}{V_O} + \frac{R_S P_O}{V_O} + V_O \tag{6}$$

after which we derive the Taylor series expansion [8] and approximate the linear equation as

$$V_s \approx V_{SO} + s^2 L_S C_f \Delta V_O + sR_S C_f \Delta V_O - s\frac{L_S P_O}{V_{OO}^2}\Delta V_O - \frac{R_S P_O}{V_{OO}^2}\Delta V_O + \Delta V_O \tag{7}$$

where V_{SO} is the nominal source voltage, ΔV_O is the small signal variation in output voltage and V_{OO} is the nominal DC output voltage value of V_O. In order to achieve a transfer function, which is a ratio of output to input, we manipulate the terms of the Taylor series expansion in (7) to get

$$V_S - V_{SO} = \Delta V_S \approx s^2 L_S C_f \Delta V_O + sR_S C_f \Delta V_O - \frac{sL_S P_O}{V_{OO}^2}\Delta V_O - \frac{R_S P_O}{V_{OO}^2}\Delta V_O + \Delta V_O \tag{8}$$

where ΔV_S is the small signal variation in source voltage. Simplifying (8), we get

$$\frac{\Delta V_O}{\Delta V_S} = \frac{1}{s^2 L_S C_f + s\left(R_S C_f - \frac{L_S P_O}{V_{OO}^2}\right) + \left(1 - \frac{R_S P_O}{V_{OO}^2}\right)} \tag{9}$$

By examining the roots of (9), we can determine the requirements for stability, which can be seen from the requirements that

$$R_S C_f - \frac{L_S P_O}{V_{OO}^2} > 0 \tag{10}$$

and

$$1 - \frac{R_S P_O}{V_{OO}^2} > 0 \tag{11}$$

for stable operation [6]. When solving (10) for L_S and (11) for R_S, we can better understand what measures need to be taken to ensure stability. To ensure stable operation, the coefficients of the characteristic equation must be positive; this ensures that the poles end up in the left-half plane. Rearranging (10) and (11), we get, respectively,

$$R_S C_f - \frac{L_S P_O}{V_{OO}^2} > 0 \Rightarrow R_S C_f > \frac{L_S P_O}{V_{OO}^2} \Rightarrow L_S < \frac{V_{OO}^2}{P_O} R_S C_f \tag{12}$$

and

$$1 - \frac{R_S P_O}{V_{OO}^2} > 0 \Rightarrow 1 > \frac{R_S P_O}{V_{OO}^2} \Rightarrow R_S < \frac{V_{OO}^2}{P_O}. \tag{13}$$

In order to maintain stability in an ideal CPL, one must carefully choose the source resistance and the source inductance. Looking back at equation (9) allows one to identify the components that, when varied, affect system stability.

By solving the roots of the characteristic equation, we were able to predict the stability of the system when using specific components. The three coefficients of the second order polynomial that is the characteristic equation of the system are represented by

$$H_{i\_vec} = \left[L_S C_f \quad R_S C_f - \left(\frac{L_S Poi}{Voo^2} \right) \quad 1 - \left(\frac{R_S Poi}{Voo^2} \right) \right] \tag{14}$$

for the initial load or power level (*Poi*) and

$$H_{f\_vec} = \left[L_S C_f \quad R_S C_f - \left(\frac{L_S Pof}{Voo^2} \right) \quad 1 - \left(\frac{R_S Pof}{Voo^2} \right) \right] \tag{15}$$

for the final load or power level (*Pof*) which is higher than the initial power level. Equations (14) and (15) were evaluated in Matlab.

1. Frequency Domain Plots

When L_S or C_f are varied in equations (14) and (15), the solutions to the characteristic equation, the poles, move as shown in Figures 5, 6 and 7. These values are better known as the roots or eigenvalues of the system.

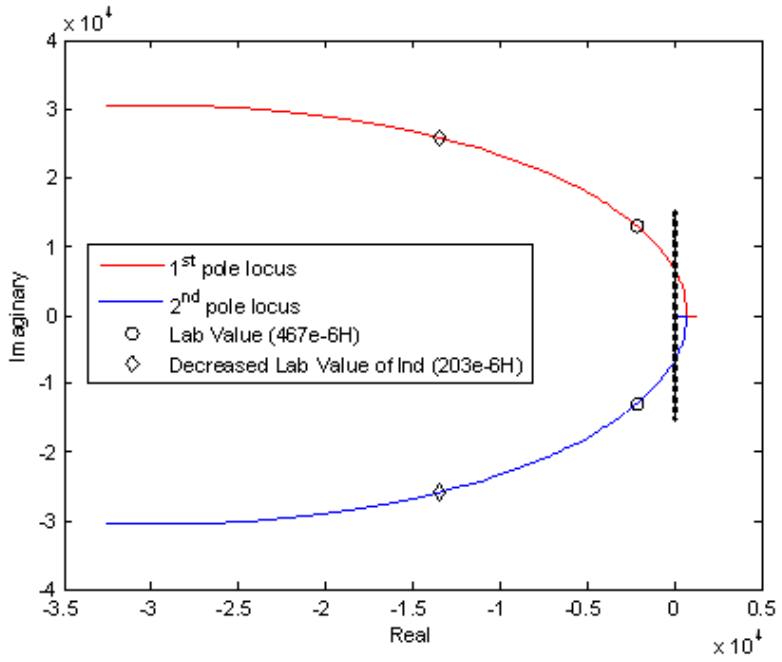

Figure 5. Root locus plot holding C_f constant and varying L_S at the initial power level.

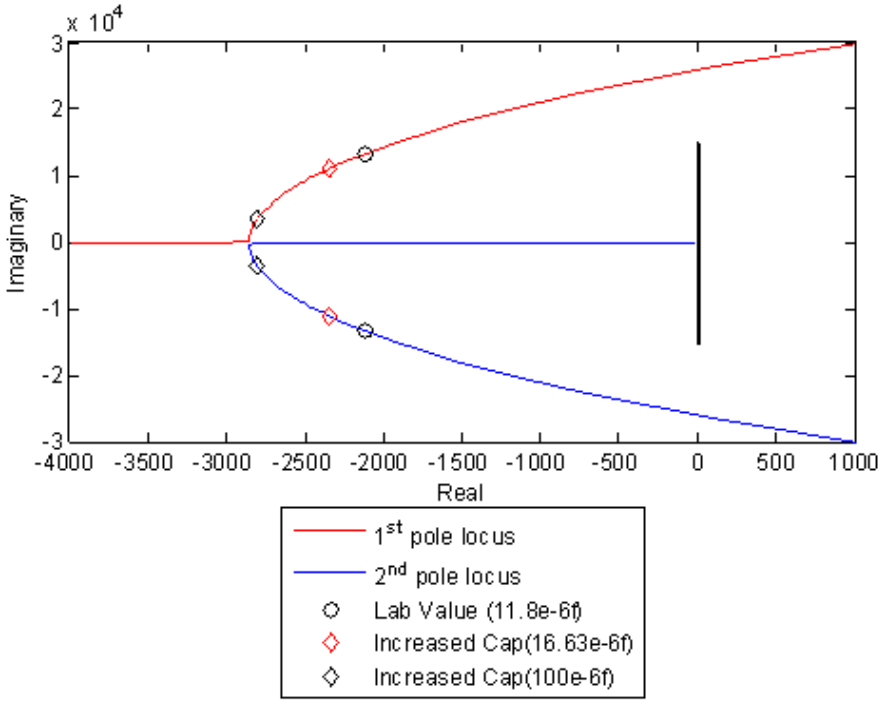

Figure 6. Root locus plot holding L_S constant and varying C_f at the initial power level.

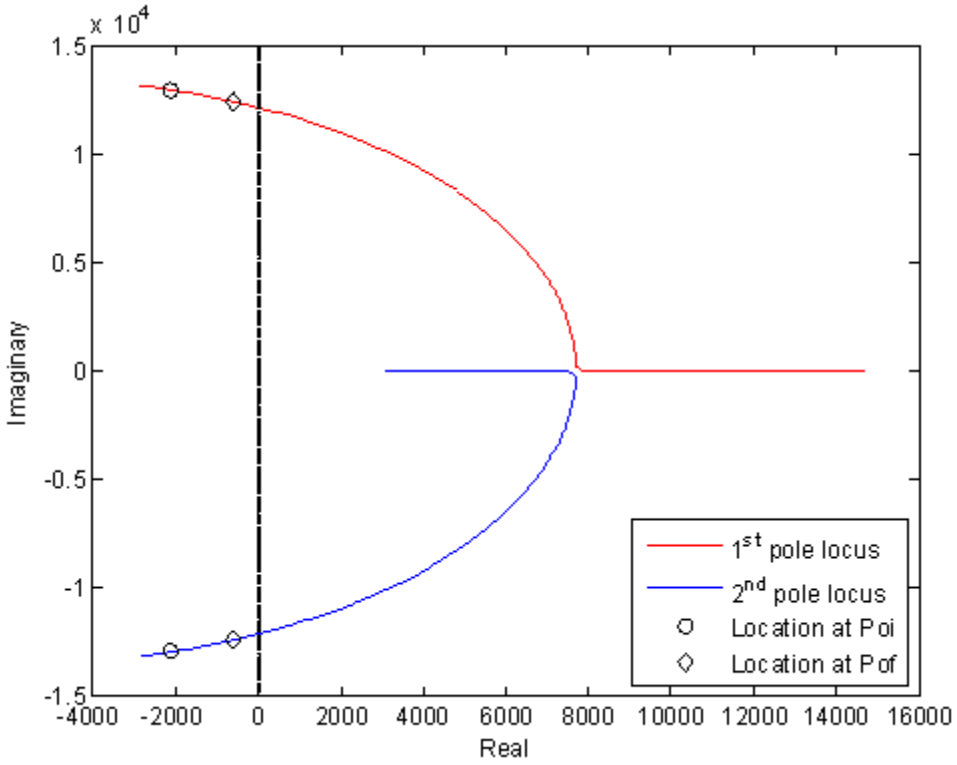

Figure 7. Root locus plot for varying load/ power level with initial C_f and L_S.

As the inductance L_S decreases and all other components remain the same, the system becomes more stable as shown in Figure 5. As the capacitance is increased and all other components remain the same, the system becomes more stable as shown in Figure 6. As the power level is increased and all other components remain the same, the system becomes more unstable as shown in Figure 7. Figures 6 and 7 are consistent with the findings of the Simulink model of the CPL and the hardware experiment which are compared in the results section. The simulation predicted the frequency and gain which can be compared to the lab measurements. The frequency can be compared between the nonlinear simulation, the linearized transfer function and the measured data. The amplitude of the input disturbance in the nonlinear simulation and in the lab measurements is unknown. Due to the unknown input disturbance, the gain from the transfer function cannot be compared to the disturbance output from the nonlinear simulation and the measured data because we do not know the amplitude of the input (or source) noise of the circuit.

C. HARDWARE MODEL

A simple model was constructed in order to compare the simulation results with the laboratory experimental results. A PROTO-BOARD PB-503 was used for the construction of the circuit, and the built-in power supply was used as the source V_S. Two capacitors, two inductors, and two resistors were used, and the Power-one was used as the buck converter.

The Power-one is a power electronics converter. The specific model used was a DC-DC step-down converter. Because of trade secrets or intellectual property, the specific components or control methods that are being used are unknown. The Power-one application document does show a high level block diagram that includes a transformer and a buck converter with what looks to be a closed loop control of current which is probably designed to tightly regulate the output voltage.

The circuit that was used to build the hardware experiment is shown in Figure 8. The values and specifics of the components used are shown in Table 1. The switch is how the load was changed from the initial to the final. When the switch was closed, R_1 and R_2 were in parallel so the resistance decreases. From equation (1), as the resistance decreases, the power increases. Therefore, as R decreases the load, or power level, increases.

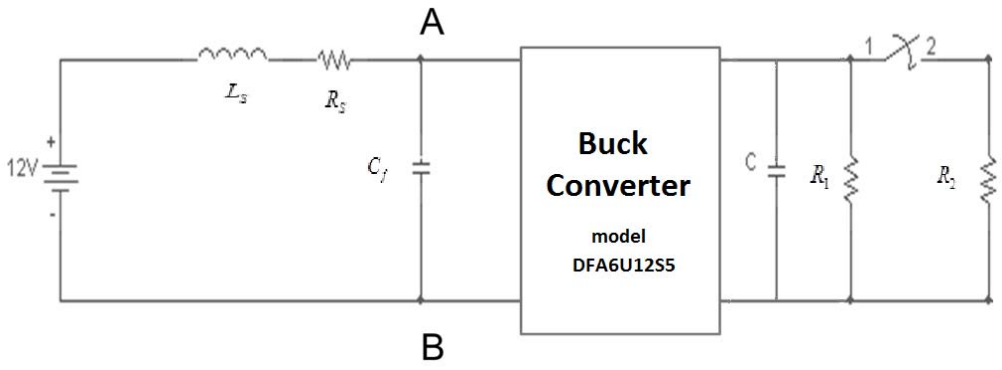

Figure 8. Diagram of hardware experiment. All measurements were taken from nodes AB, channel two on oscilliscope screenshots

Table 1. Values used in hardware experiment

	Original Values (Measured)	Values to see effects on Stability (Measured)
Calming/filter Capacitor (C_f) EPCOS 12 μF K 630V-MKP	11.8μF	First value 16.63μF Final value 100μF
Inductor (L_S) 1130-471-RC	467μH	203μH (Two 1130-471-RC in ‖)
Power level (Resistor value) R1: YAGEO-DGK 10W 10 Ω J R2: YAGEO-DGK 10W 4.7 Ω J	R1: 10.02 Ω	R1 ‖ R2 : 4.65 Ω
Noise reduction Capacitor (C) EPCOS 20 μF K 450V-MKP	19.5μF	19.5μF

A picture of my laboratory experiment is shown in Figure 9. The inductor was connected to the PROTO-BOARD and one of the capacitors was placed in series with it. Then the positive input terminal of the buck converter was connected to the positive lead of the capacitor. The negative terminals of both the buck converter and capacitor were connected to ground which put the buck converter in parallel with the capacitor. This step is necessary in order to allow the capacitor to act as a filter capacitor to help make the system more stable. The resistors are in parallel and are connected to the output terminal of the buck converter as stated above and as shown in Figure 8. Again, the switch is what allowed for the load change. The final capacitor (C) was to help reduce system noise as suggested by the buck converter application notes and does not affect stability.

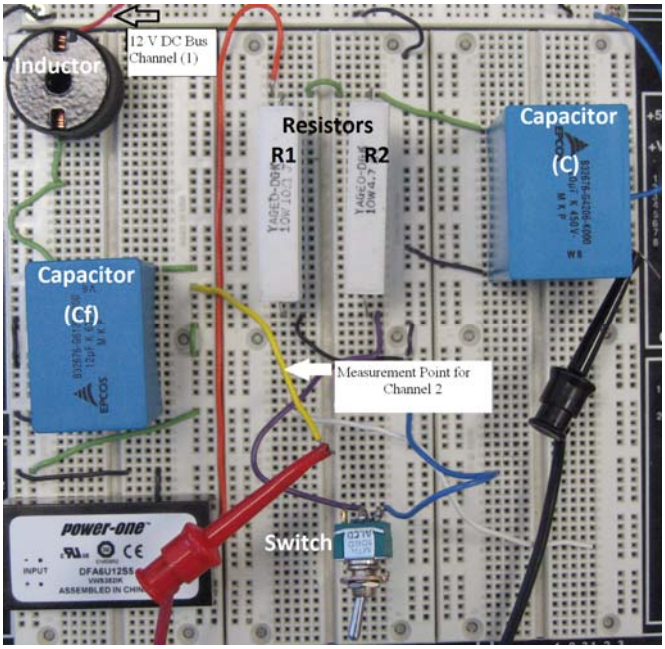

Figure 9. Picture of hardware experiment

The different methods used to examine the stability of a circuit with a CPL were discussed in this chapter. The simulation method, which in this thesis was Matlab's Simulink program, was introduced first. Then the linearized equation of the idealized CPL model was developed, and the stability requirements from the linearized equations were introduced. The last thing discussed in this chapter was the hardware model that is used to verify the two previous methods for predicting stability. The results from all three methods of analysis are discussed in the next chapter.

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IV. RESULTS

Changing the input source impedance affected whether the system became more or less stable. Ways in which the Simulink model, the linearized equation of the ideal nonlinear model, and the hardware experiment show similar characteristics, and ways in which the frequency of the disturbance on the bus feeding the CPL at the initial power level are similar are discussed in this chapter. The frequency of the disturbance is not predicted as well at the higher power level, which might be due to the internal components of the Power-one module and the control measures it uses to maintain a constant voltage. We did not know what the control measures were and cannot better determine the exact cause.

A. INITIAL LOAD COMPARISON WITH CHANGING L_S

The behavior at the initial power level (*Poi*) and decreasing the value of L_S are analyzed in this section. For ease of review, the results from the different methods of analysis are shown in Tables 2 and 3.

Table 2. $L_S = 467\mu H$ at initial load

	Simulink Plot	Transfer function analysis	Hardware verification
Frequency	2000 Hz	2037.2 Hz	1950 Hz
Amplitude (Gain dB)	21.16 V	10.2 dB	13.1 V

Table 3. $L_S = 203\mu H$ at initial load.

	Simulink Plot	Transfer function analysis/Bode	Hardware verification
Frequency	3333 Hz	2881 Hz	2980 Hz
Amplitude (Gain dB)	9.52 V	5.35 dB	11.9 V

It can be seen from Tables 2 and 3 that, as inductance was decreased, the system becomes more stable. The frequency increases and the amplitude or gain decreases.

From either Table 2 or Table 3 it can be seen that all three methods of analyses predicted approximately the same frequency.

Figure 10 and Figure 11 are the plots from the Simulink model of the ideal CPL. When comparing Figure 10 to Figure 11, we can see that the amplitude is decreasing and the frequency of the disturbance on the bus feeding the CPL is increasing. The following plots represent the data that was taken to make Tables 2 and 3.

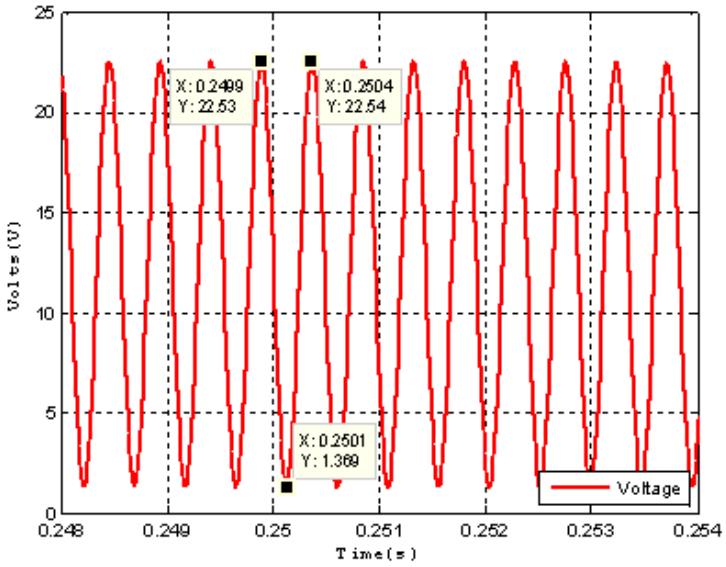

Figure 10. Capacitor Voltage for constant power load with $L_S = 467\mu H$ at *Poi*.

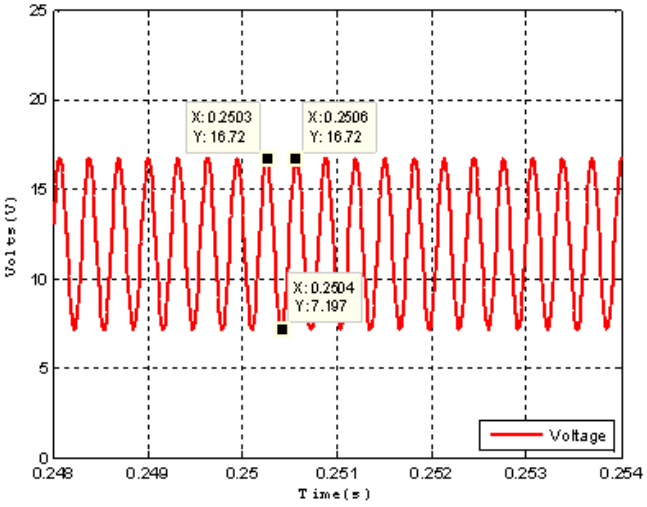

Figure 11. Capacitor Voltage for constant power load with $L_S = 203\mu H$ at *Poi*.

In Figure 12, as the inductance decreases and the poles move further into the left-half plane, the system becomes more stable. These results are consistent with the information in Tables 2 and 3. In Figures 13 and 14, the frequency is given in radians per second, and in Tables 2 and 3 the frequency is given in Hz; the conversion is made by dividing the Bode plot freqency by 2π. The gain in Figures 13 and 14 also decreases which indicates that the system is becoming more stable and is consistant with Tables 2 and 3.

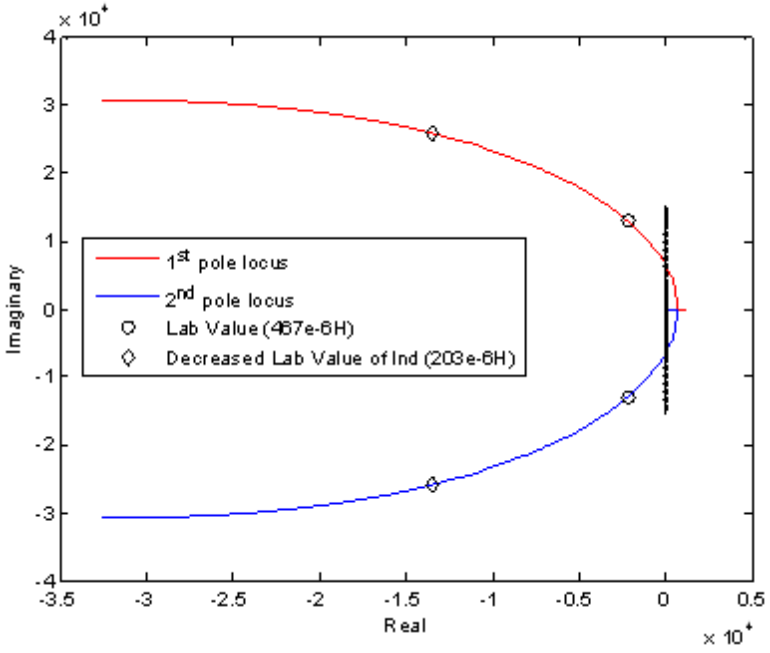

Figure 12. Stability plot at *Poi* holding C_f constant and varying L_S

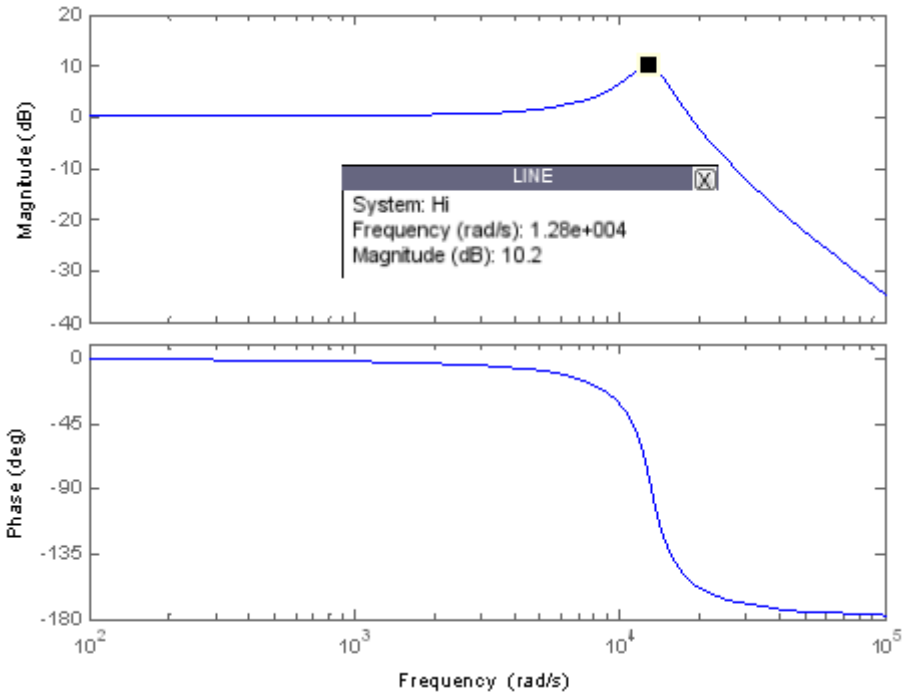

Figure 13. Bode plot for $L_S = 467\mu H$ at *Poi*.

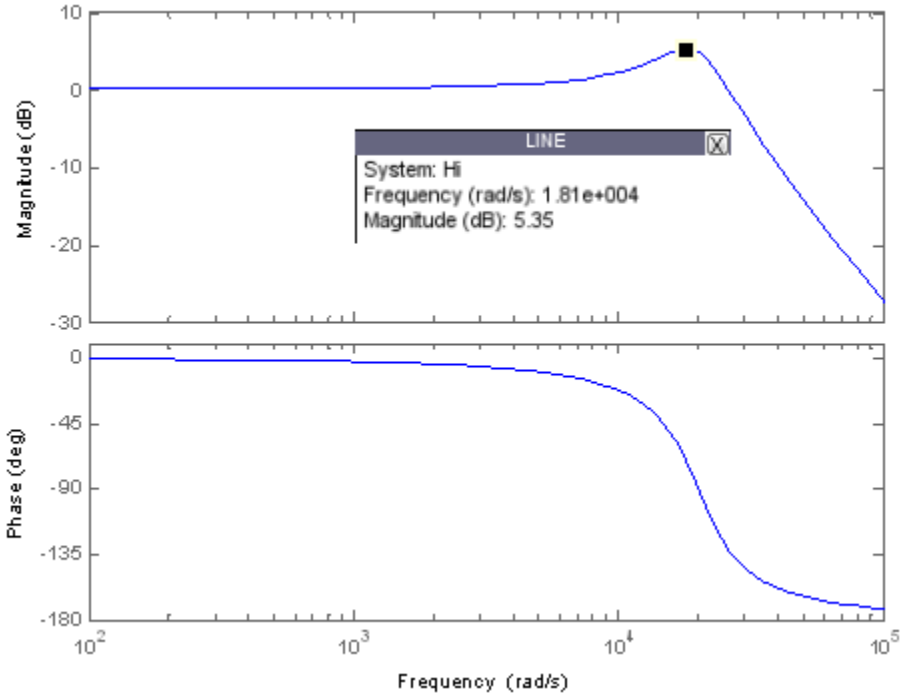

Figure 14. Bode plot for $L_S = 203\mu H$ at *Poi*.

Figures 15 and 16 are oscilloscope screenshots from the hardware experiment showing the input voltage to the CPL. When comparing Figure 15 to Figure 16, we can see that the frequency increases and the amplitude decreases, as shown in Tables 2 and 3.

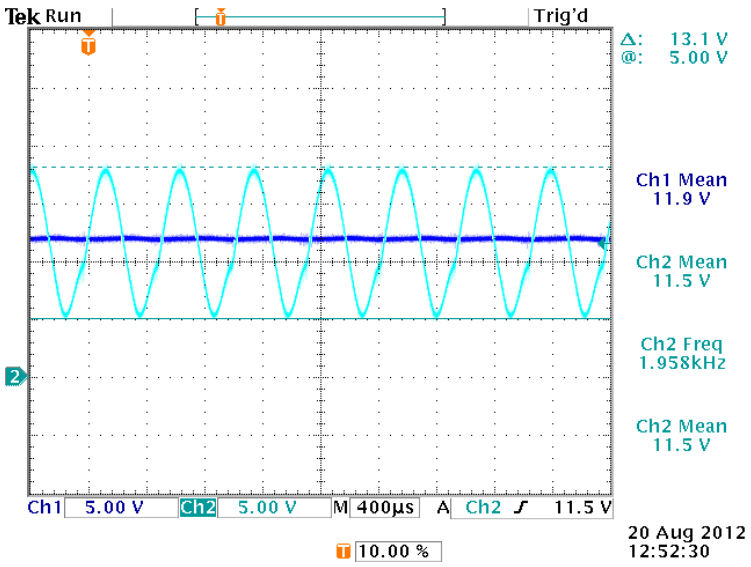

Figure 15. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with $L_S = 467\mu H$ at *Poi*. Amplitude = 13.1 V and frequency = 1950 Hz measured with cursors.

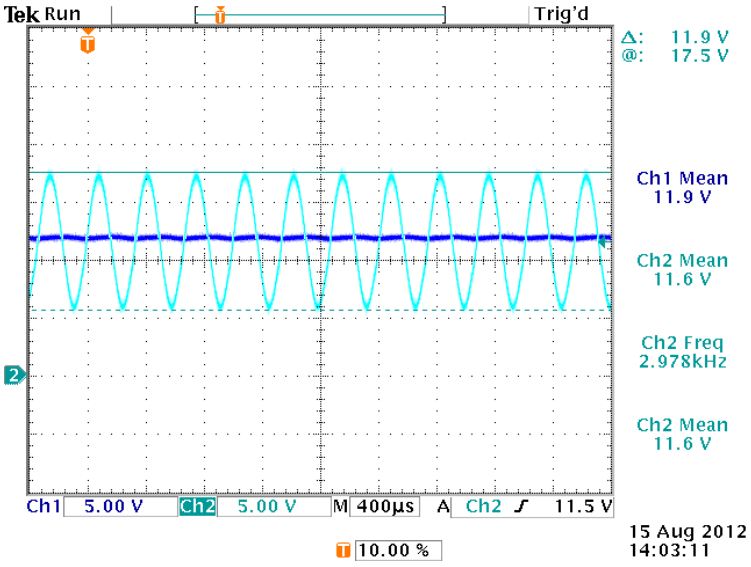

Figure 16. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with $L_S = 203\mu H$ at *Poi*. Amplitude = 11.9 V and frequency = 2980 Hz measured with cursors.

B. FINAL LOAD COMPARISON WITH CHANGING L_S

The behavior at a higher power level (*Pof*) compared to the previous section while decreasing the value of L_S is analyzed in this section. For ease of review, the results from the different methods of analysis are shown in Tables 4 and 5.

Table 4. $L_S = 467\mu H$ at final load.

	Simulink Plot	Transfer function analysis/Bode	Hardware verification
Frequency	2000 Hz	1973.5 Hz	2080 Hz
Amplitude (Gain dB)	13.11 V	22.1 dB	14.2 V

Table 5. $L_S = 203\mu H$ at final load.

	Simulink Plot	Transfer function analysis/Bode	Hardware verification
Frequency	2500 Hz	2833 Hz	3050 Hz
Amplitude (Gain dB)	5.76 V	8.38 dB	13.9 V

It can be seen from Tables 4 and 5 that again, as the inductance decreases, the system becomes more stable even when operating at a higher power level. All three methods of analyses again predict similar trends. Frequency is not as well predicted as in the initial load, possibly because of the unknown control methods of the buck converter and how it reacts at higher power level demands.

Figure 17 and Figure 18 are the plots from the Simulink model of the ideal CPL. When comparing Figure 17 to Figure 18, we can see that the amplitude is decreasing and the frequency increasing. The following plots represent the data taken to make Tables 4 and 5.

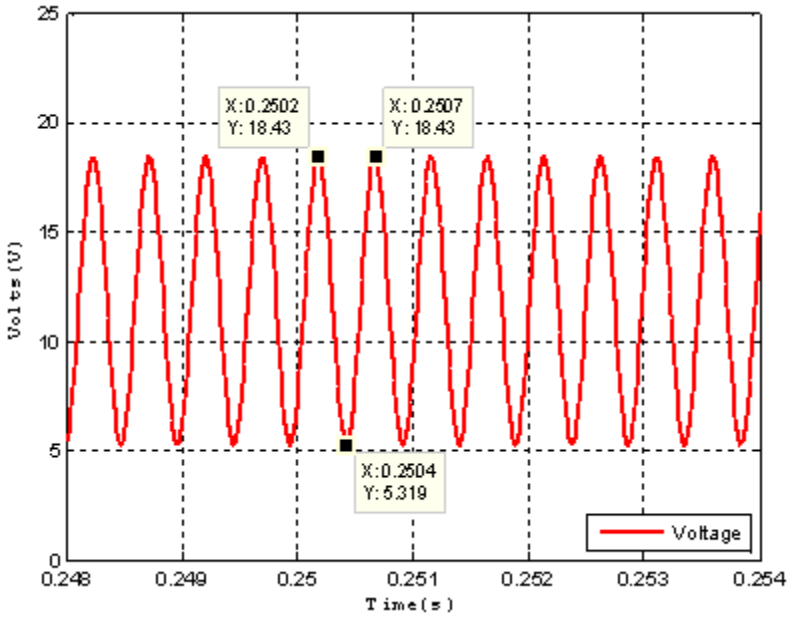

Figure 17. Capacitor Voltage for constant power load with $L_S = 467\mu H$ at *Pof*.

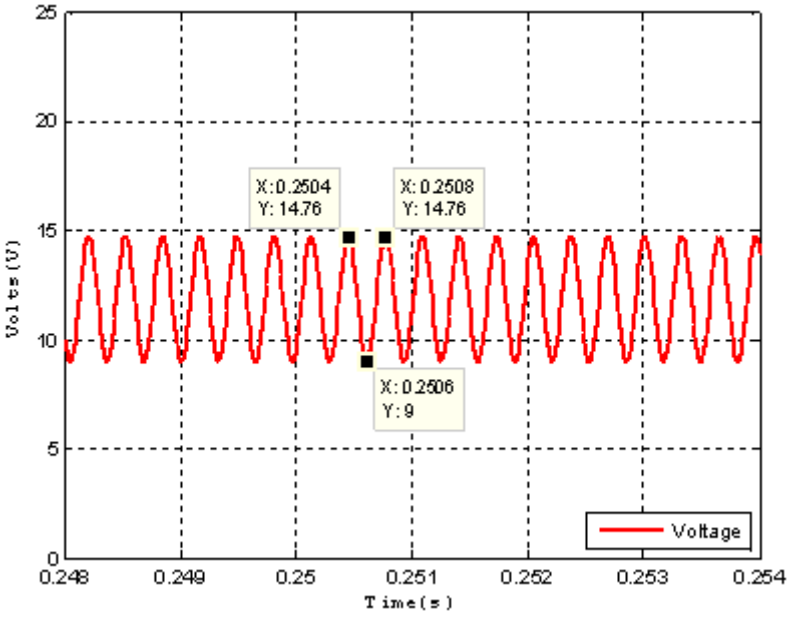

Figure 18. Capacitor Voltage for constant power load with $L_S = 203\mu H$ at *Pof*.

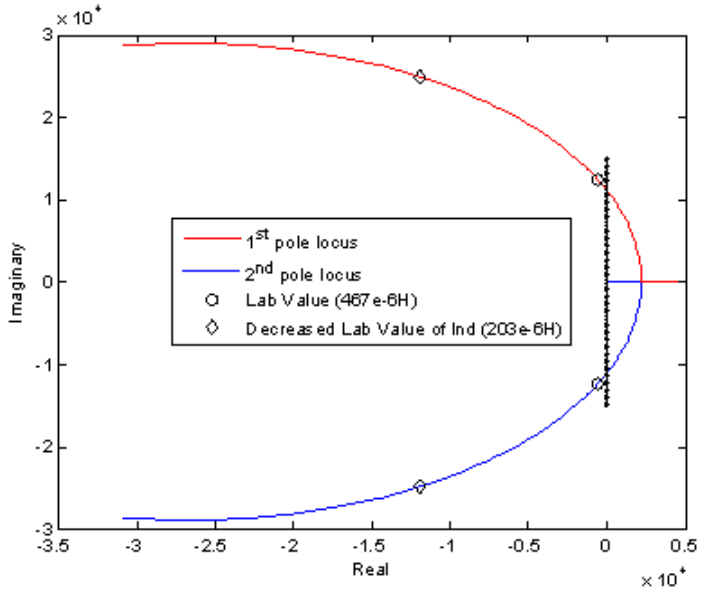

Figure 19. Stability plot at *Pof* holding C_f constant and varying L_S

In Figure 19, as the inductance decreases and the poles move further into the left-half plane, the system becomes more stable. These results are consistent with the information in Tables 4 and 5. The gain in Figures 20 and 21 also decreases, which indicates that the system is becoming more stable and is consistant with Tables 4 and 5.

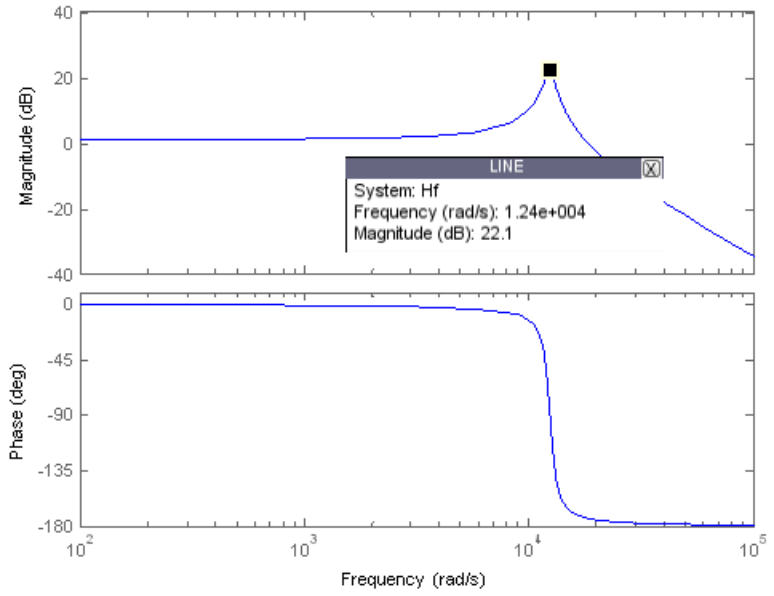

Figure 20. Bode plot with $L_S = 467\mu H$ at the final load

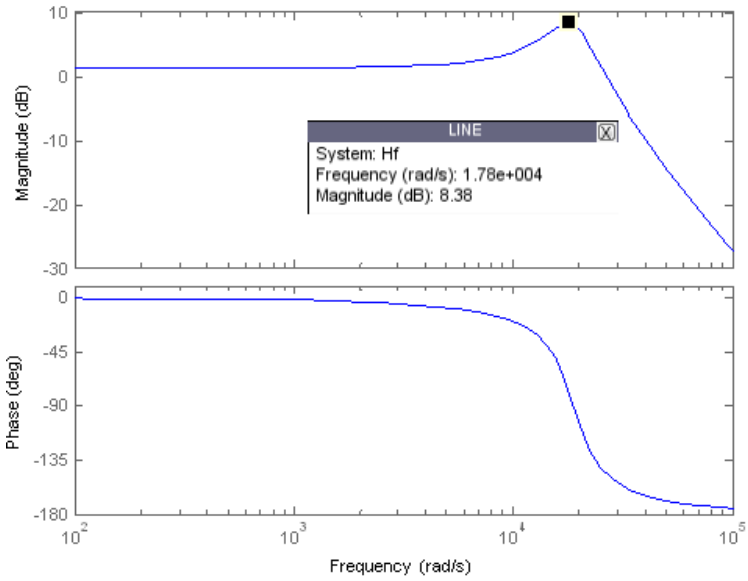

Figure 21. Bode plot for $L_S = 203\mu H$ at the final load

Figures 22 and 23 are oscilloscope screenshots from the hardware experiment. When comparing Figure 22 to Figure 23, we can see that the frequency increases and the amplitude decreases, as shown in Tables 4 and 5.

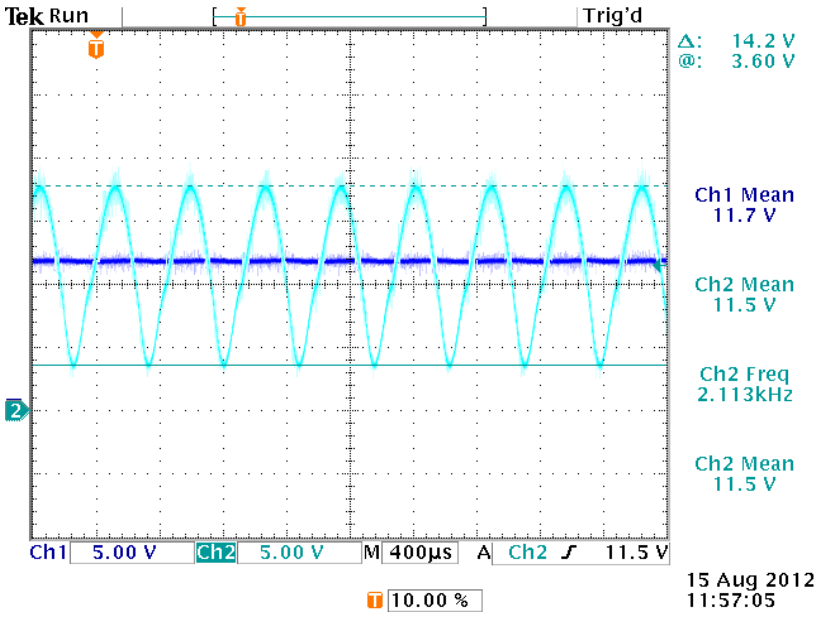

Figure 22. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with $L_S = 467\mu H$ at *Pof*. Amplitude = 14.2V and frequency =2080 Hz measured with cursors

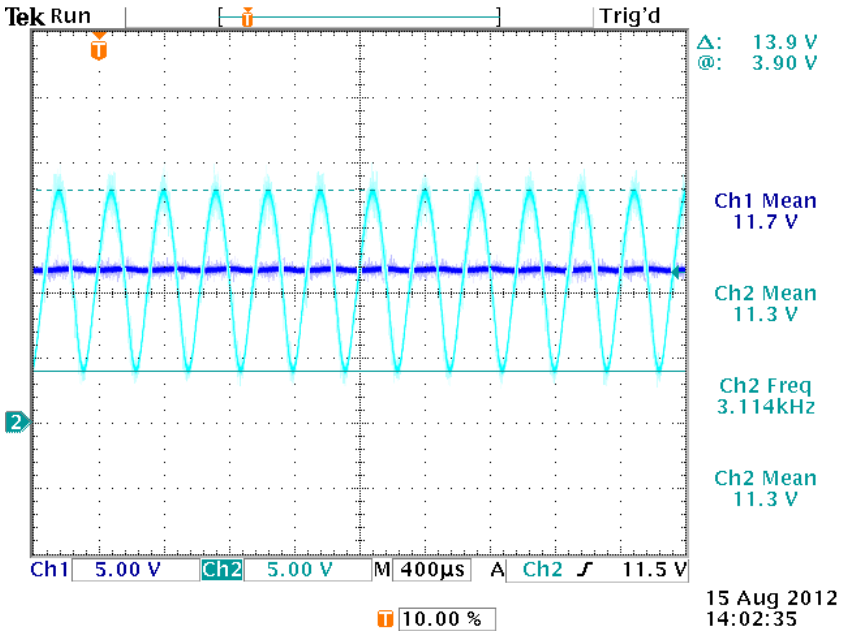

Figure 23. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with $L_S = 203\mu H$ at *Pof*. Amplitude = 13.9 V and frequency = 3050 Hz measured with cursors

C. INITIAL LOAD COMPARISON WITH CHANGING C_f.

The behavior at the initial power level while increasing the value of C_f is analyzed in this section. For ease of review, the results from the different methods of analysis are shown in Tables 6 and 7.

Table 6. $C_f = 11.8\mu$F at initial load.

	Simulink Plot	Transfer function analysis	Hardware verification
Frequency	2000 Hz	2037.2 Hz	1950 Hz
Amplitude (Gain dB)	21.16 V	10.2 dB	13.0 V

Table 7. C_f = 16.63μF at initial load

	Simulink Plot	Transfer function analysis/Bode	Hardware verification
Frequency	1666 Hz	1687 Hz	1710 Hz
Amplitude (Gain dB)	20.36 V	7.99 dB	12.2 V

It can be seen from Tables 6 and 7 that, as the capacitance increases, the system becomes more stable. All three methods of analyses predict approximately the same frequency at the initial load.

Figure 24 and Figure 25 are the plots from the Simulink model of the ideal CPL. When comparing Figure 24 to Figure 25, we can see that the amplitude and frequency are decreasing. The following plots represent the data that was taken to make Tables 6 and 7.

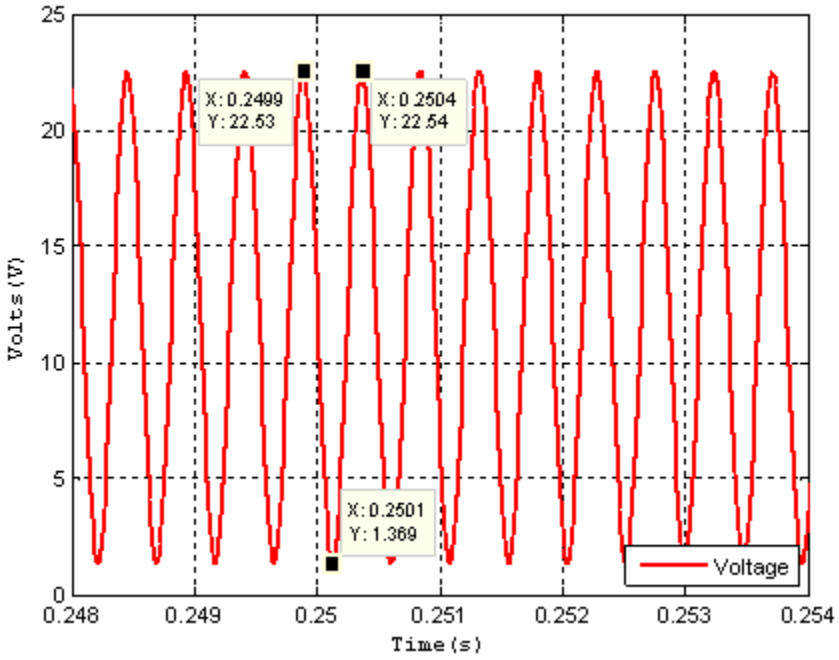

Figure 24. Capacitor voltage for constant power load with C_f = 11.8μF

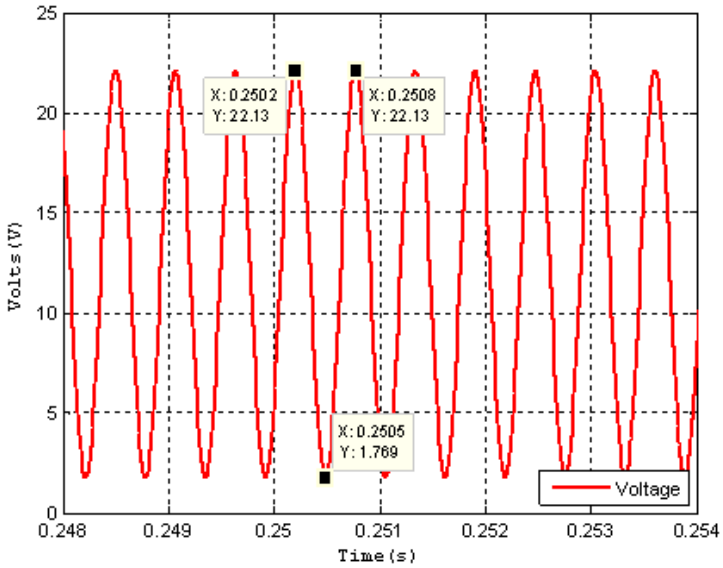

Figure 25. Capacitor voltage for constant power load with C_f = 16.63μF.

In Figure 26, as the capacitance increases and the poles move further into the left-half plane, the system becomes more stable. These results are consistent with the information in Tables 6 and 7. The gain in Figures 27 and 28 is also decreasing, which indicates that the system is becoming more stable, consistant with Tables 6 and 7.

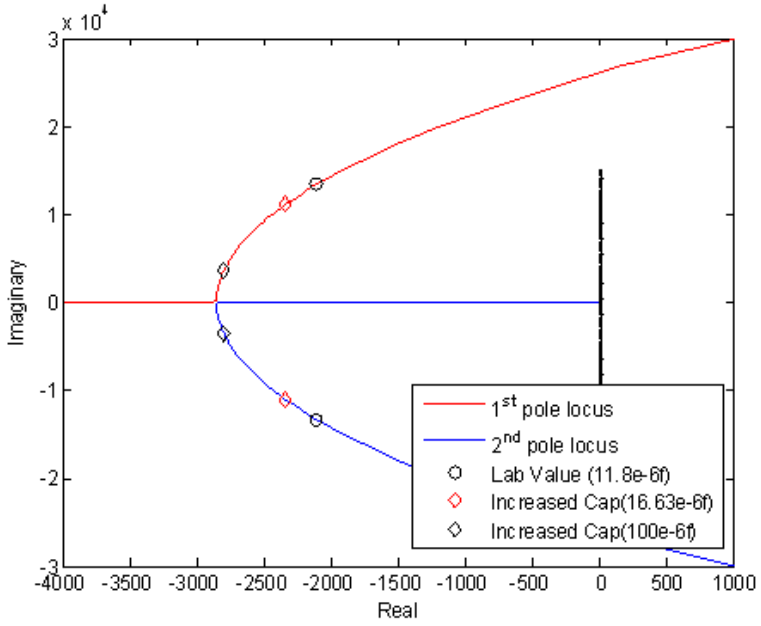

Figure 26. Stability plot holding L_S constant and varying C_f at the initial load.

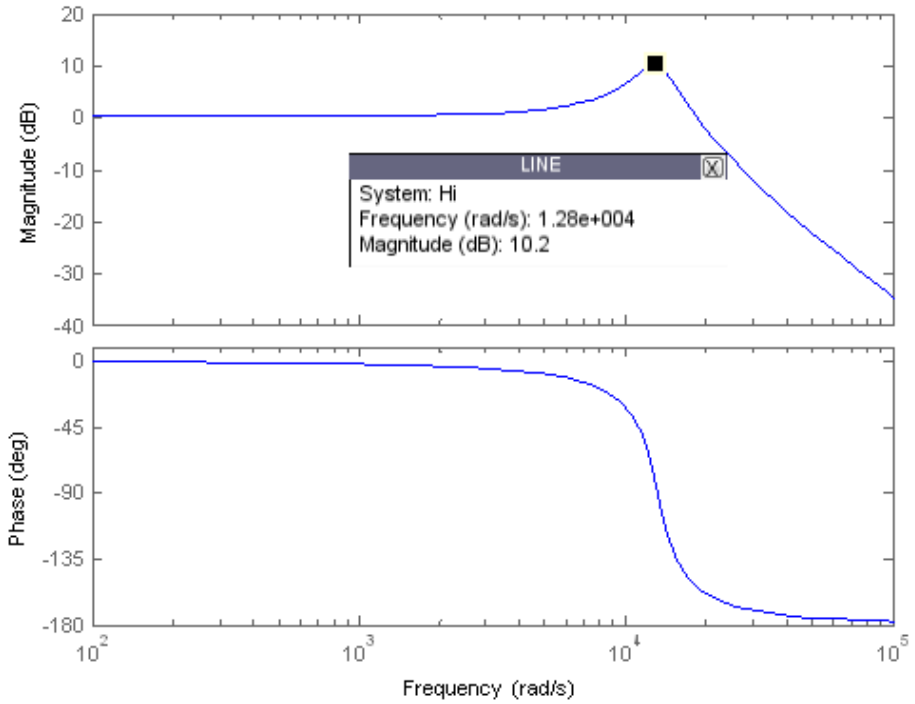

Figure 27. Bode plot with C_f = 11.8μF at the initial load.

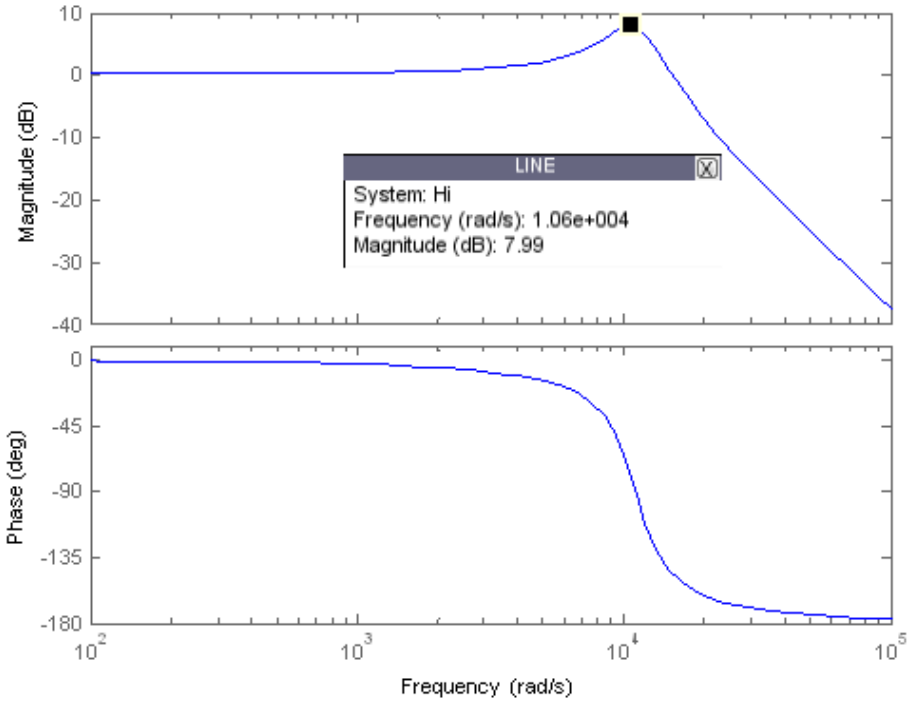

Figure 28. Bode plot with C_f = 16.63μF at the initial load.

Figures 29 and 30 are oscilloscope screenshots from the hardware experiment. When comparing Figure 29 to Figure 30, we can see that the amplitude and frequency are decreasing, as shown in Tables 4 and 5 when the capacitance was increased.

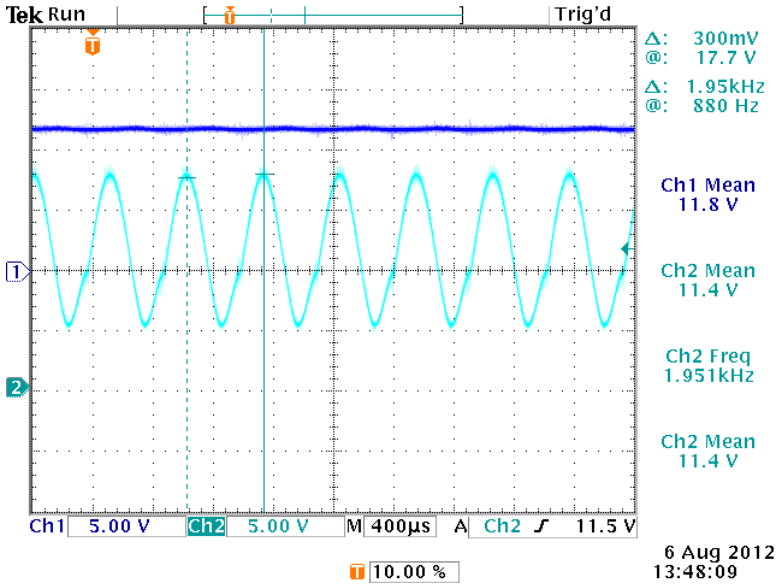

Figure 29. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with C_f = 11.8μF *Poi*. Amplitude = 13V and frequency =1950 Hz measured with cursors.

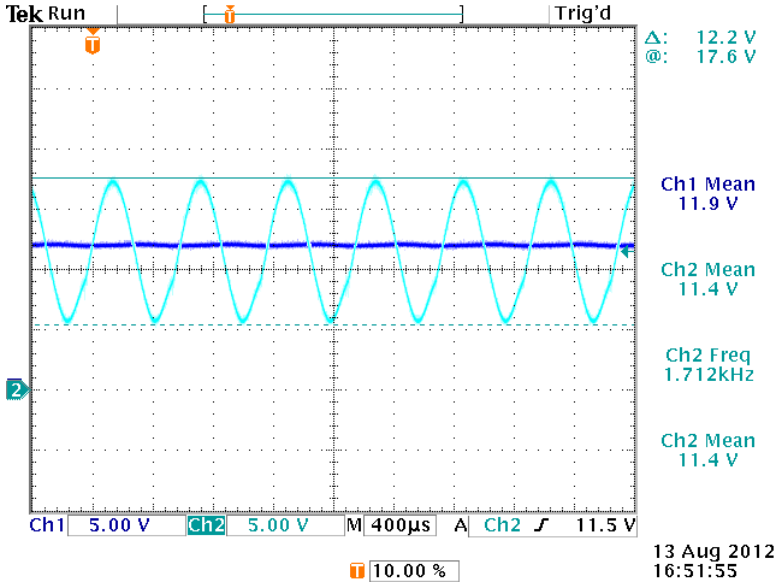

Figure 30. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with C_f = 16.63μF at *Poi*. Amplitude = 12.2V and frequency = 1710 Hz measured with cursors.

D. FINAL LOAD COMPARISON VARYING C_f

The behavior at a higher power level compared to the previous section while increasing the value of C_f is analyzed in this section. For ease of review, the results from the different methods of analysis are shown in Tables 8 and 9.

Table 8. $C_f = 11.8\mu F$ at final load

	Simulink Plot	Transfer function analysis/Bode	Hardware verification
Frequency	2000 Hz	1973.5 Hz	2160 Hz
Amplitude (Gain dB)	13.11 V	22.1 dB	14.0 V

Table 9. $C_f = 16.63\mu F$ at final load.

	Simulink Plot	Transfer function analysis/Bode	Hardware verification
Frequency	2000 Hz	1639 Hz	1790 Hz
Amplitude (Gain dB)	13.01 V	13.9 dB	13.0 V

It can be seen from Tables 8 and 9 that, as the capacitance increases, the system becomes more stable. All three methods of analyses again predict similar trends. Frequency is not as well predicted as for the initial load, which could be due to the unknown control methods of the buck converter and how it reacts at higher power levels.

Figure 31 and Figure 32 are the plots from the Simulink model of the ideal CPL. When comparing Figure 31 to Figure 32, we can see that the amplitude and frequency are decreasing. The following plots represent the data that was taken to make Tables 8 and 9.

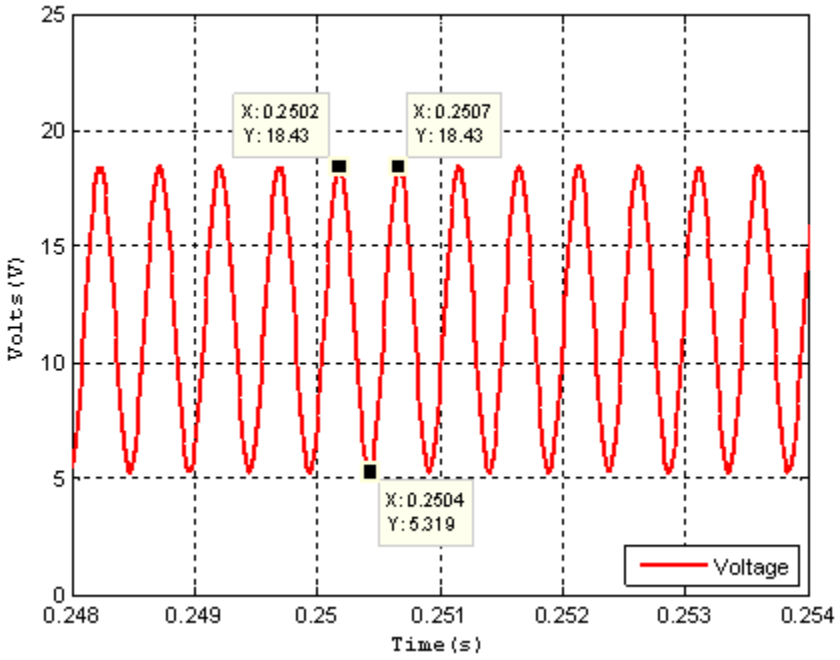

Figure 31. Capacitor voltage for constant power load with C_f = 11.8μF.

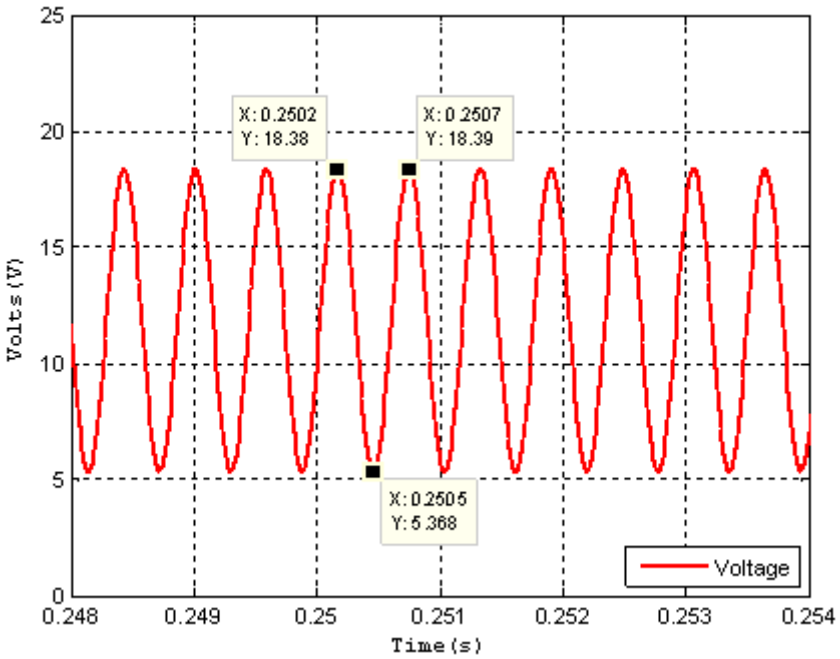

Figure 32. Capacitor voltage for constant power load with C_f = 16.63μF.

In Figure 33, as the capacitance increases and the poles move further into the left-half plane, the system becomes more stable. These results are consistent with the information in Tables 8 and 9. The gain in Figures 34 and 35 is also decreasing, which indicates that the system is becoming more stable, consistant with Tables 8 and 9.

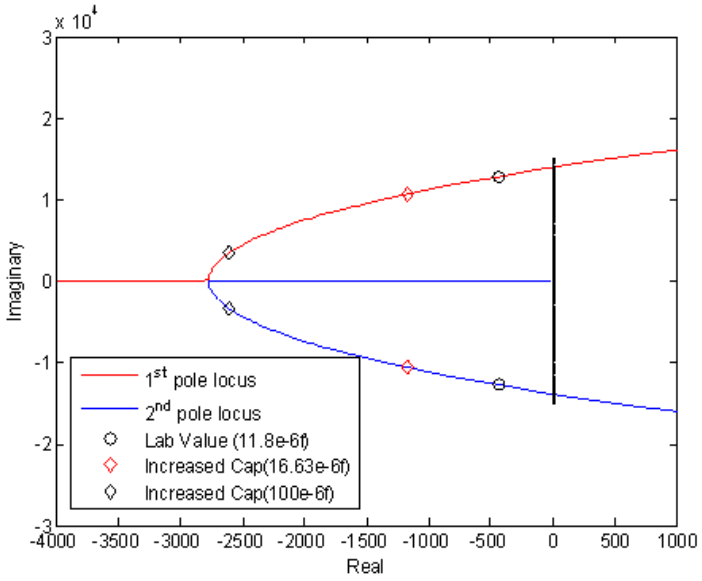

Figure 33. Stability plot holding L_S constant and varying C_f at the final load.

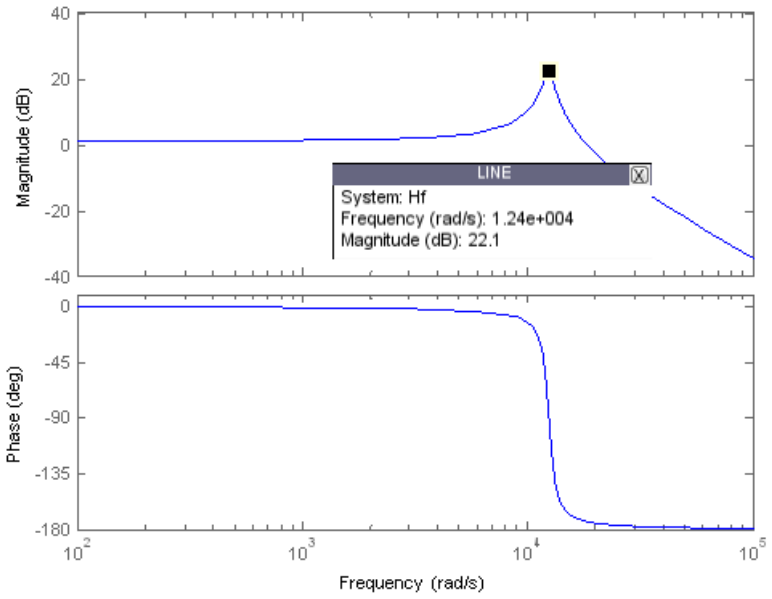

Figure 34. Bode plot with C_f = 11.8μF at the final load.

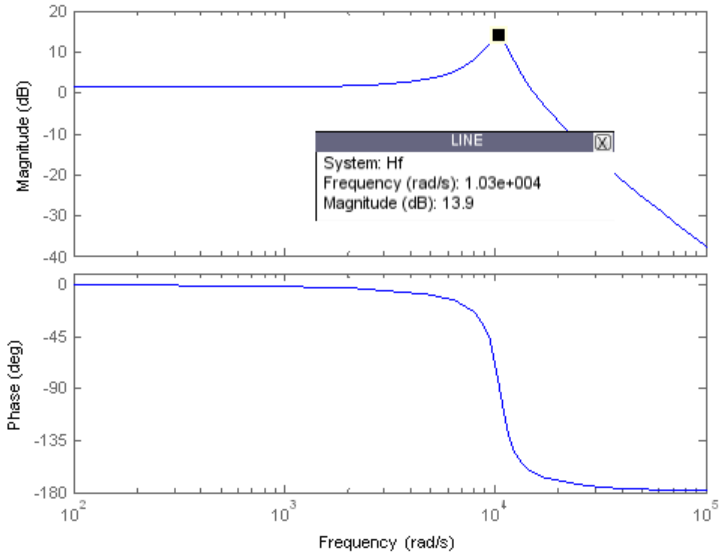

Figure 35. Bode plot with C_f = 16.63μF at the final load.

Figures 36 and 37 are oscilloscope screenshots from the hardware experiment. When comparing Figure 36 to Figure 37, we can see that the amplitude and frequency are decreasing, as shown in Tables 8 and 9 as the capacitance increased.

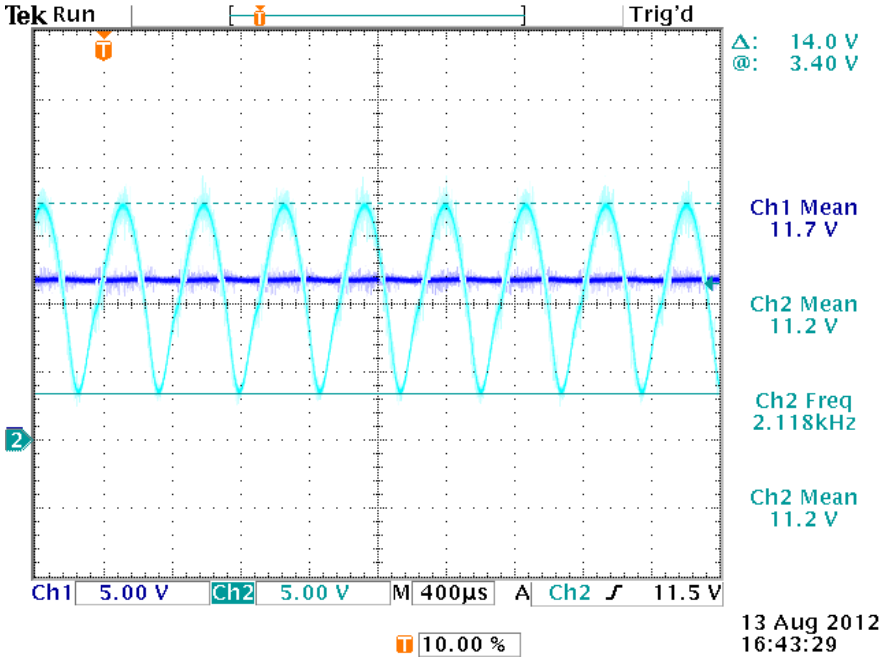

Figure 36. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with C_f = 11.8μF at final load. Amplitude = 14.0 V and frequency = 2160 Hz measured with cursors.

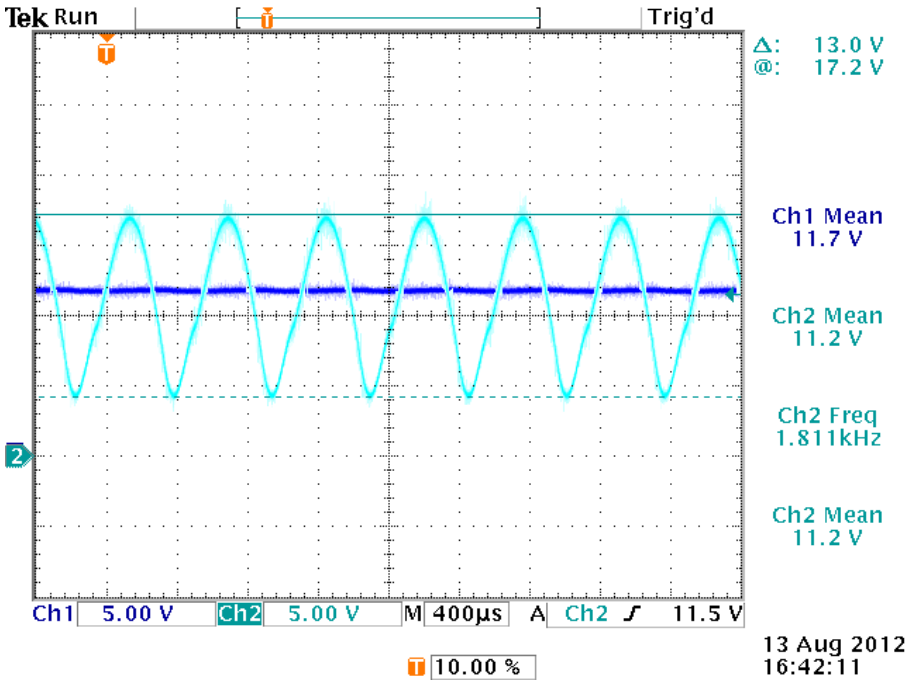

Figure 37. Oscilloscope screen capture of CPL input voltage (ch2) and source voltage (ch1) with C_f = 16.63μF at final load. Amplitude = 13.0 V and frequency = 1790 Hz measured with cursors.

E. ROOT LOCUS ANALYSES FOR VARYING LOAD RESISTANCE.

Figures 38–41 are root locus plots when varying the load resistance or power level. In Figure 38, the roots with the original component values at the initial and final power levels as a starting point are shown. In Figure 39, a root locus plot with L_S decreased at the initial and final power levels is shown. In Figure 40, a root locus plot with C_f increased at the initial and final power levels is shown. In Figure 41, a root locus plot when C_f was increased and L_S was decreased at the initial and final power levels is shown. From these plots we conclude that the load of the system affected the stability of the system independent of the source impedance, and that changing the source impedance helped stabilize the system.

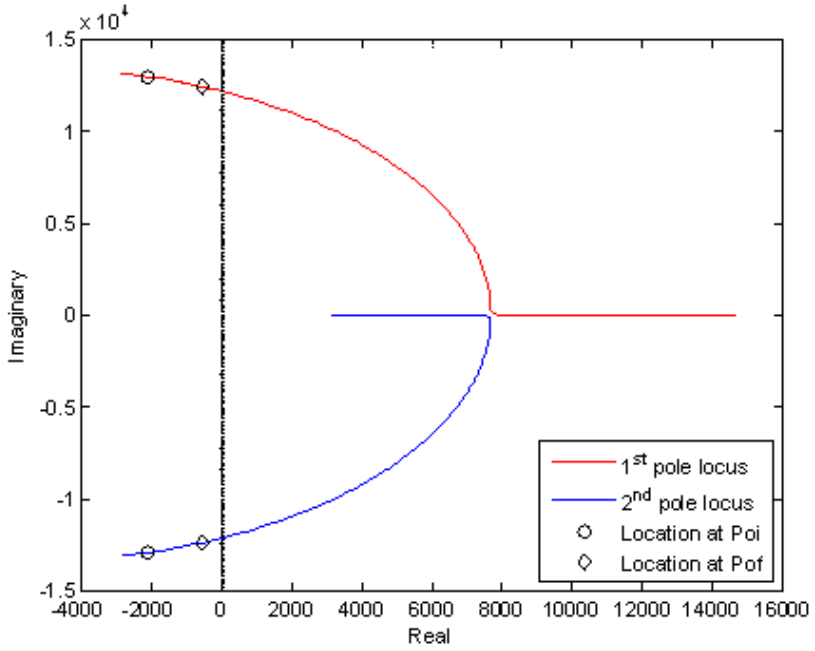

Figure 38. Stability plot with $L_S = 467\mu H$ and $C_f = 11.8\mu$F.

As the load or power level increases, the system becomes less stable as the poles move closer to the right-half plane as shown in Figure 38.

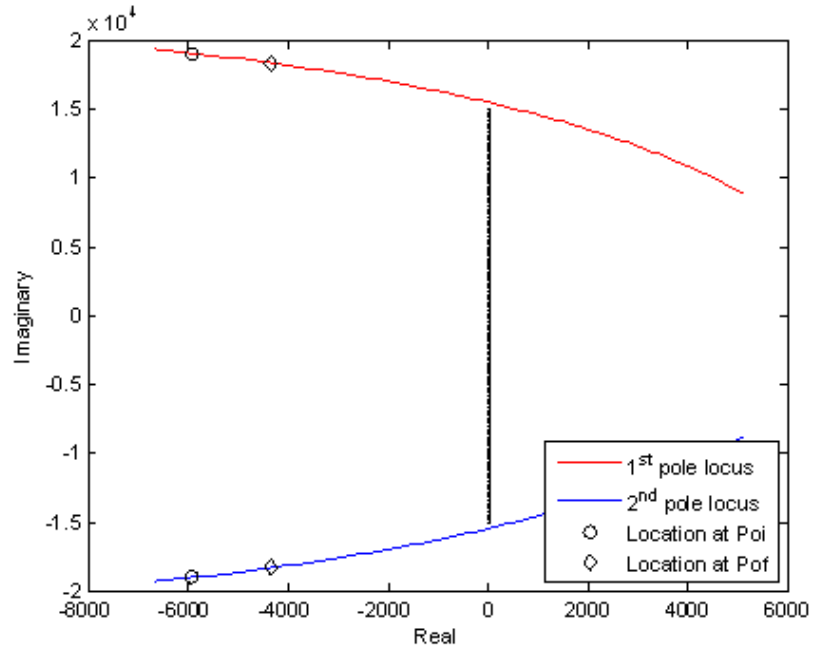

Figure 39. Stability plot with $L_S = 203\mu H$ and $C_f = 11.8\mu F$.

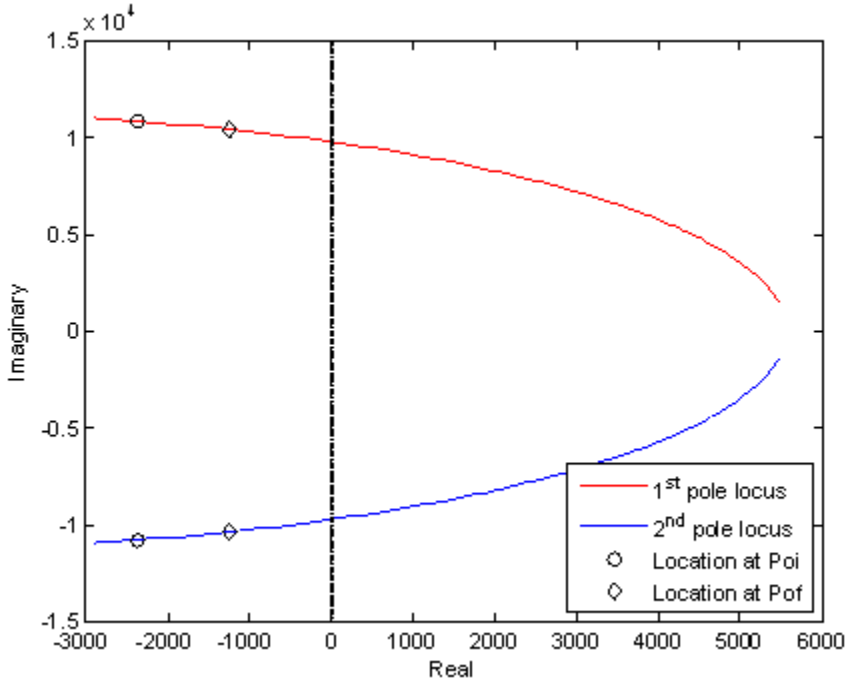

Figure 40. Stability plot with $L_S = 467\mu H$ and $C_f = 16.63\mu F$.

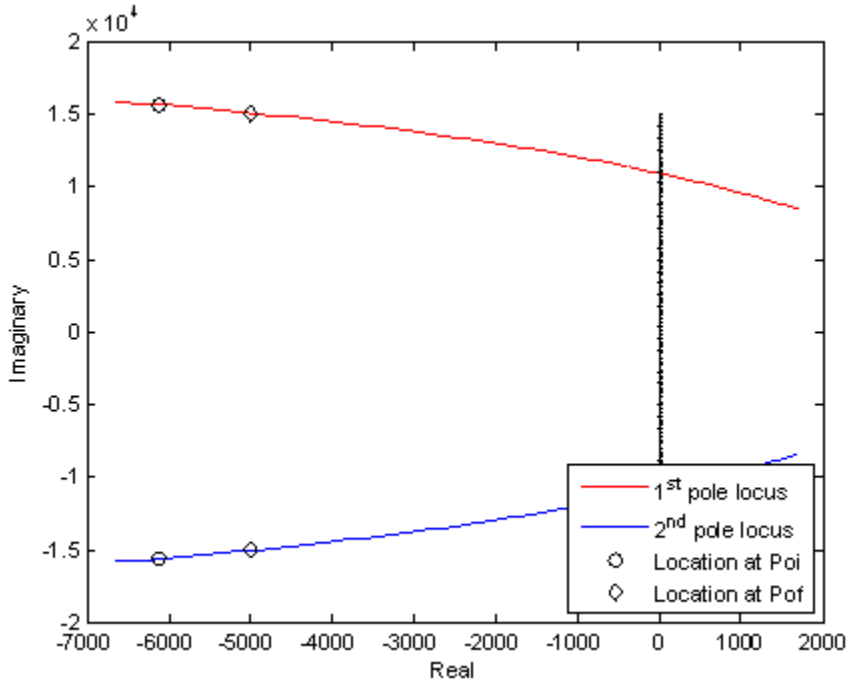

Figure 41. Stability plot with $L_S = 203\mu$ H and $C_f = 16.63\mu F$.

The effects of changing L_S and C_f were discussed in this chapter. When L_S and C_f are changed in the appropriate ways to improve stability the roots moved further away from the right-half plane as shown in Figures 39, 40 and 41. The figures from the previous sections validated the root locus' prediction of stability as the load changed and as the inductance and capacitance changed. When increasing the capacitance and decreasing the inductance at the same time as shown in Figure 41, the poles of the system moved further into the left-half plane than when only changing L_S or C_f independently as shown in Figures 39 and 40. The overall findings of how changing the source impedance affected the systems stability is discussed in the next chapter. A few recommendations are also made on how this thesis' work could be improved to allow for better stability prediction.

V. CONCLUSIONS AND RECOMMENDATIONS

A. ACCOMPLISHMENTS

The characteristic trait of tightly regulated power electronics which act like CPLs and the stability issues concerning CPLs were reviewed in this thesis. A Simulink model of an ideal CPL was used, along with a linearized model of the nonlinear ideal Simulink model, to predict the stability of the system as the input source impedance varied. A hardware experiment was built in the lab using a commercial off-the-shelf DC –DC converter to act as a CPL. This model was a simple, hands-on model of the Simulink model, used to verify the predictions of both the ideal model and the linearized model.

The results observed showed that the models accurately predicted the frequency of the hardware experiment at the initial load. The amplitude was not accurately predicted at either load, but the trend was similar for all three methods of analyses. The frequency at the final load was also not accurately predicted, but again the same trend was seen in all methods of analyses. The buck converter's control scheme is not known; this unknown factor may explain the inaccurate prediction at higher loads.

B. FUTURE WORK

An ideal Simulink model was used. The model is not as accurate as real-world systems; however, systems are designed to be as close to ideal as possible. The Simulink model used a slew rate limiter to control the rate of change of the commanded current. The linearized equation which was used to find the roots of the characteristic equation and plot the findings did not incorporate the slew rate limiter. A change that would allow a more accurate representation would be to replace the slew rate limiter in the Simulink model with a low pass filter, which can be modeled as a transfer function and added into the linearized equation.

Another opportunity for further work would be to replace the Power-one module and its unknown control scheme with a DC-DC converter for which the control scheme is known. Knowing the control scheme of the DC-DC converter, the researcher would have the ability to more accurately validate the models.

It was noted that the amplitude of the input disturbance for steady state operation is not known for the nonlinear simulation and the lab measurements. Future work could look at the step response to try to estimate the eigenvalues from the nonlinear simulations and lab measurements.

APPENDIX MATLAB CODE

This Appendix contains the Matlab code used to analyze the data received from the Simulink model. The Matlab code used to analyze the linearized equation of the ideal constant power of the circuit in Figure 3. It also contains the Matlab code used to generate all the plots found in this thesis.

```
%Stability_ic.m
%LT George Roth Sep 2012
Rs=.18; % for Ls = 467e-6
Ls=467e-6;
%Ls=203e-6; %increased value to show effect on stability
Cf=11.8e-6;
%Cf = 16.63e-6; %increased to show effect on stability
Vdc=12;

%Stability_plot.m

time=simout(:,3);
current=simout(:,1);
voltage=simout(:,2);
figure(8);
%plot(time,current,'b','linewidth',2)
%hold on;
plot(time,voltage,'r','linewidth',2)
hold off;
xlabel('Time(s)','FontName','FixedWidth')
ylabel('Volts(V)','FontName','FixedWidth')
axis([.248 .254 0 25]);
grid;
legend('Voltage','Location','SouthEast');
title('Capacitor Voltage for constant power load');
%title('Capacitor Voltage and Source current for constant current
load');

%Analysis.m
clear,clc
close all
Ls = 467e-6; % original value
%Ls = 203e-6; % decreased value to show affect on stability
Rs = .18*15; % Multiply by 15 to take into account for unknown
resistance in protoboard.
%Cf = 11.8e-6; % original value from lab.
Cf = 16.63e-6; % Increased Capacitor value from lab to show affects on
Stability.
V = 5; %Voltage
R1 = 10.02; %Resistor one
R2 = 4.65; %Resistor two
Ri = R1; % Initial Resistance
Rf = R1*R2/(R1+R2); %Final Resistance
Poi = V^2/Ri; %Initial Power
```

```
Pof = V^2/Rf; %Final Power
Voo = 12; %Nominal output voltage

%%%%%   Finding roots of characteristic equation
Hi_vec=[Ls*Cf (Rs*Cf-(Ls*Poi)/Voo^2) (1-(Rs*Poi)/Voo^2)]
Hi = tf([1],Hi_vec)
Hf_vec=[Ls*Cf (Rs*Cf-(Ls*Pof)/Voo^2) (1-(Rs*Pof)/Voo^2)]

Hf = tf([1],Hf_vec)

char_roots_i = roots(Hi_vec)
char_roots_f = roots(Hf_vec)

% complex number = a +jomega and omega = 2*pi*f so:
% r1 = 13439.09671;
% r2 = 13235.3212;
% f_i = r1/(2*pi)
% f_f = r2/(2*pi)


%%%%    Plotting roots of characteristic equation for different values
of
%%%%    Cf and Ls
Cfv = Cf/7:Cf/10:Cf*8000; %
Cfv = Cfv';
I = ones(length(Cfv),1);
Lc = [Ls*Cfv  (Rs*Cfv-(Ls*Poi)/Voo^2)  I*(1-(Rs*Poi)/Voo^2)];

%loop for the roots when varying Cf and holding Ls constant
L_rootsc = zeros(2,length(Lc)); %initialze place to store
for a=1:length(Lc) % how many times to run loop, length of L
    L_rootsc(:,a) = roots(Lc(a,:)); % Takes "a" row all columns of L
and puts result in all rows of "a" column.
end;
xx = 0;
yy = [-1.5e4:200:1.5e4];
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
figure(1)
plot(real(L_rootsc(1,:)),imag(L_rootsc(1,:)),'r');
hold on; plot(real(L_rootsc(2,:)),imag(L_rootsc(2,:)),'b');
plot(real(L_rootsc(1,9)),imag(L_rootsc(1,9)),'kO');
plot(real(L_rootsc(1,13)),imag(L_rootsc(1,13)),'rd');
plot(real(L_rootsc(1,84)),imag(L_rootsc(1,84)),'kd');
plot(xx,yy,'k');
legend('1^s^t pole locus','2^n^d pole locus','Lab Value (11.8e-
6f)','Increased Cap(16.63e-6f)','Increased Cap(100e-
6f)','Location','Best');
plot(real(L_rootsc(2,9)),imag(L_rootsc(2,9)),'kO');
plot(real(L_rootsc(2,84)),imag(L_rootsc(2,84)),'kd');
plot(real(L_rootsc(2,13)),imag(L_rootsc(2,13)),'rd');
hold off;
axis([-4000 1000 -30000 30000]);
title('Stability plot holding Ls constant and varying Cf')
xlabel('Real')
```

```
ylabel('Imaginary')

% loop for  the roots when varying Ls and holding Cf constant
Lsv = Ls/5:Ls/30:Ls*2000; %
Lsv = Lsv';
I = ones(length(Lsv),1);
L = [Lsv*Cf  (Rs*Cf-(Lsv*Poi)/Voo^2)  I*(1-(Rs*Poi)/Voo^2)];

Ls_roots = zeros(2,length(L)); %initialze place to store
for a=1:length(L) % how many times to run loop, length of L
    Ls_roots(:,a) = roots(L(a,:)); % right side of equation=Takes "a"
row all columns of L and puts (left side of equation) result in all
rows of "a" column.
end;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
figure(2)
plot(real(Ls_roots(1,:)),imag(Ls_roots(1,:)),'r');
hold on; plot(real(Ls_roots(2,:)),imag(Ls_roots(2,:)),'b');
plot(real(Ls_roots(1,64)),imag(Ls_roots(1,64)),'kO');
plot(real(Ls_roots(1,9)),imag(Ls_roots(1,9)),'kd');
plot(xx,yy,'k-')
legend('1^s^t pole locus','2^n^d pole locus','Lab Value (467e-
6H)','Decreased Lab Value of Ind (229e-6H)','Location','Best');
plot(real(Ls_roots(2,64)),imag(Ls_roots(2,64)),'kO');
plot(real(Ls_roots(2,9)),imag(Ls_roots(2,9)),'kd');
hold off;
%axis([-300 1500 -31000 31000]);
title('Stability plot at Poi holding Cf constant and varying Ls')
xlabel('Real')
ylabel('Imaginary')

% Plotting amplitude gain
figure(3)
bode(Hi)
title('Bode plot of small signal transfer function with initial load ')
axis([10e1 10e4 -180 10])

bode_freq_in_kHz_for_Hi =  1.28e4/(2*pi) % Get the numerator from the
bode plot and enter to let matlab convert, have to change everytime
% any values of initial variables are changed.

figure(4)
bode(Hf)
title('Bode plot of small signal transfer function with final load')
axis([10e1 10e4 -180 10])

bode_freq_in_kHz_for_Hf =  1.24e4/(2*pi) % Get the numerator from the
bode plot and enter to let matlab convert, have to change everytime
% any values of initial variables are changed.

%    Plotting roots of characteristic equation for different values of
%    R
Poiv = 0:.01:40;
Poiv = Poiv';
```

```
I = ones(length(Poiv),1);
Lp = [Ls*Cf*I  (Rs*Cf-(Ls*Poiv)/Voo^2)  (1-(Rs*Poiv)/Voo^2)];

% %loop for the roots when varying the power, Poi/Pof and holding Cf
and Ls constant
L_roots = zeros(2,length(Lp)); %initialze place to store
for a=1:length(Lp) % how many times to run loop, length of L
    L_roots(:,a) = roots(Lp(a,:)); % Takes "a" row all columns of L and
puts result in all rows of "a" column.
end;

figure(5)
plot(real(L_roots(1,:)),imag(L_roots(1,:)),'r');
hold on;
plot(real(L_roots(2,:)),imag(L_roots(2,:)),'b');
plot(real(L_roots(1,251)),imag(L_roots(1,251)),'kO');
plot(real(L_roots(1,788)),imag(L_roots(1,788)),'kd');
legend('1^s^t pole locus','2^n^d pole locus','Location at
Poi','Location at Pof','Location','SouthEast');
plot(real(L_roots(2,251)),imag(L_roots(2,251)),'kO');
plot(real(L_roots(2,788)),imag(L_roots(2,788)),'kd');
plot(xx,yy,'k-');
hold off;
% axis([-1000 1.5e4 -1.5e4 1.5e4]);
title('Stability plot varying Load Resistance')
xlabel('Real')
ylabel('Imaginary')
```

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